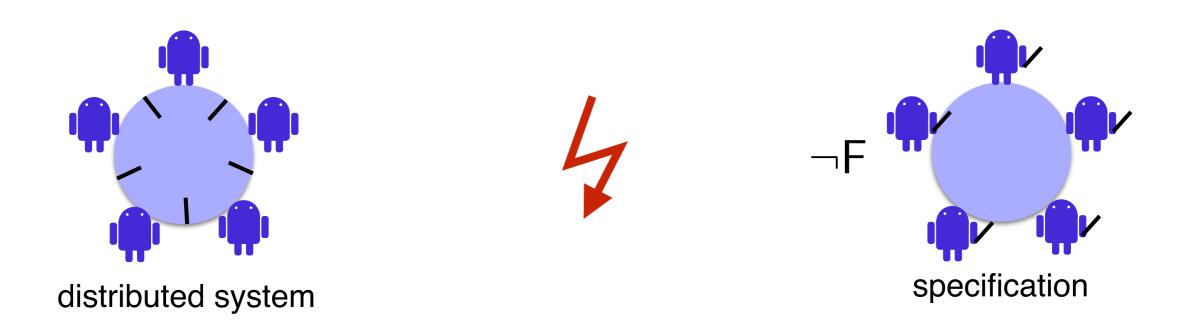
#### Formal Methods for the Verification of Distributed Algorithms

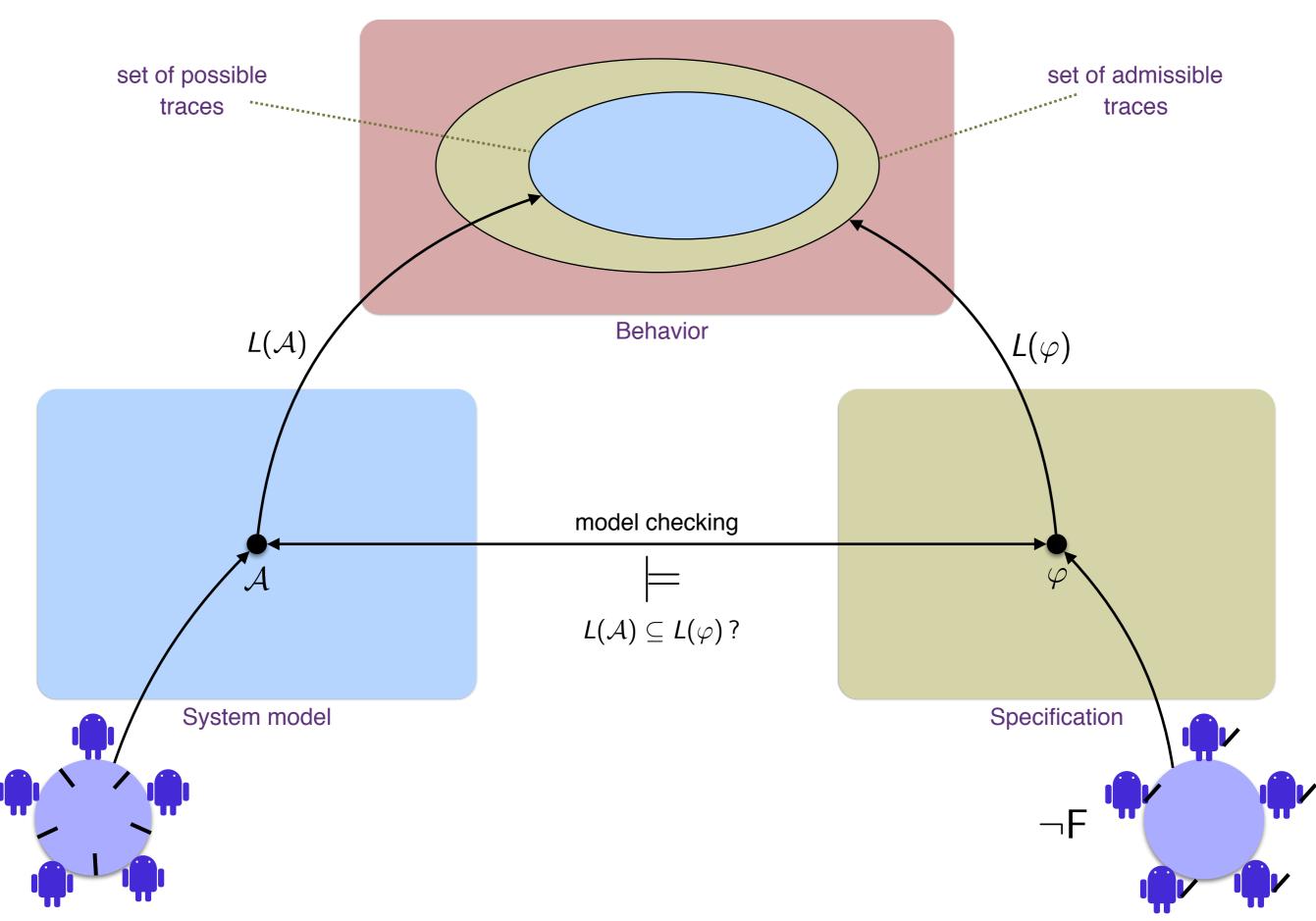
#### Paul Gastin

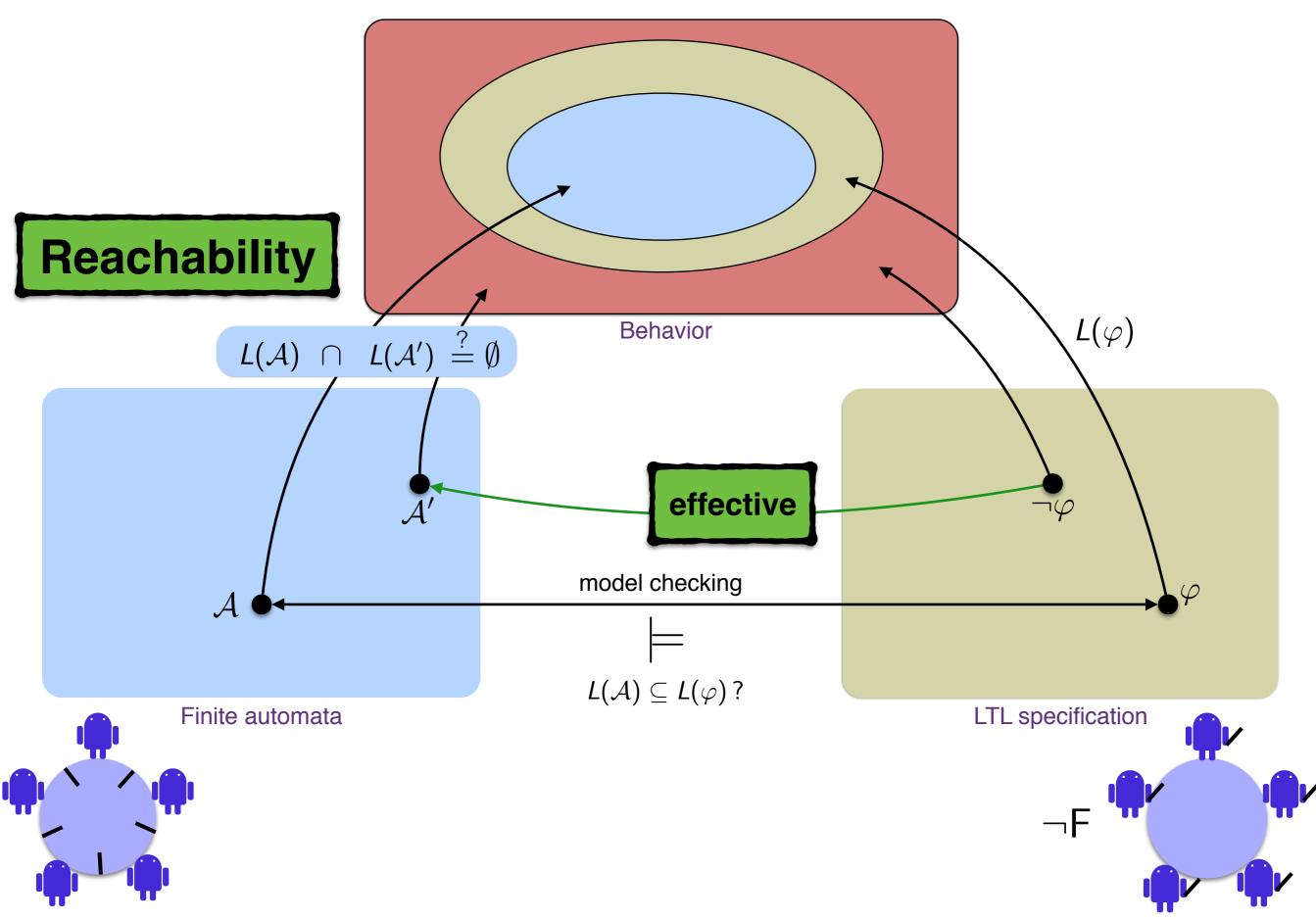
Laboratoire Spécification et Vérification ENS Cachan, CNRS & Inria

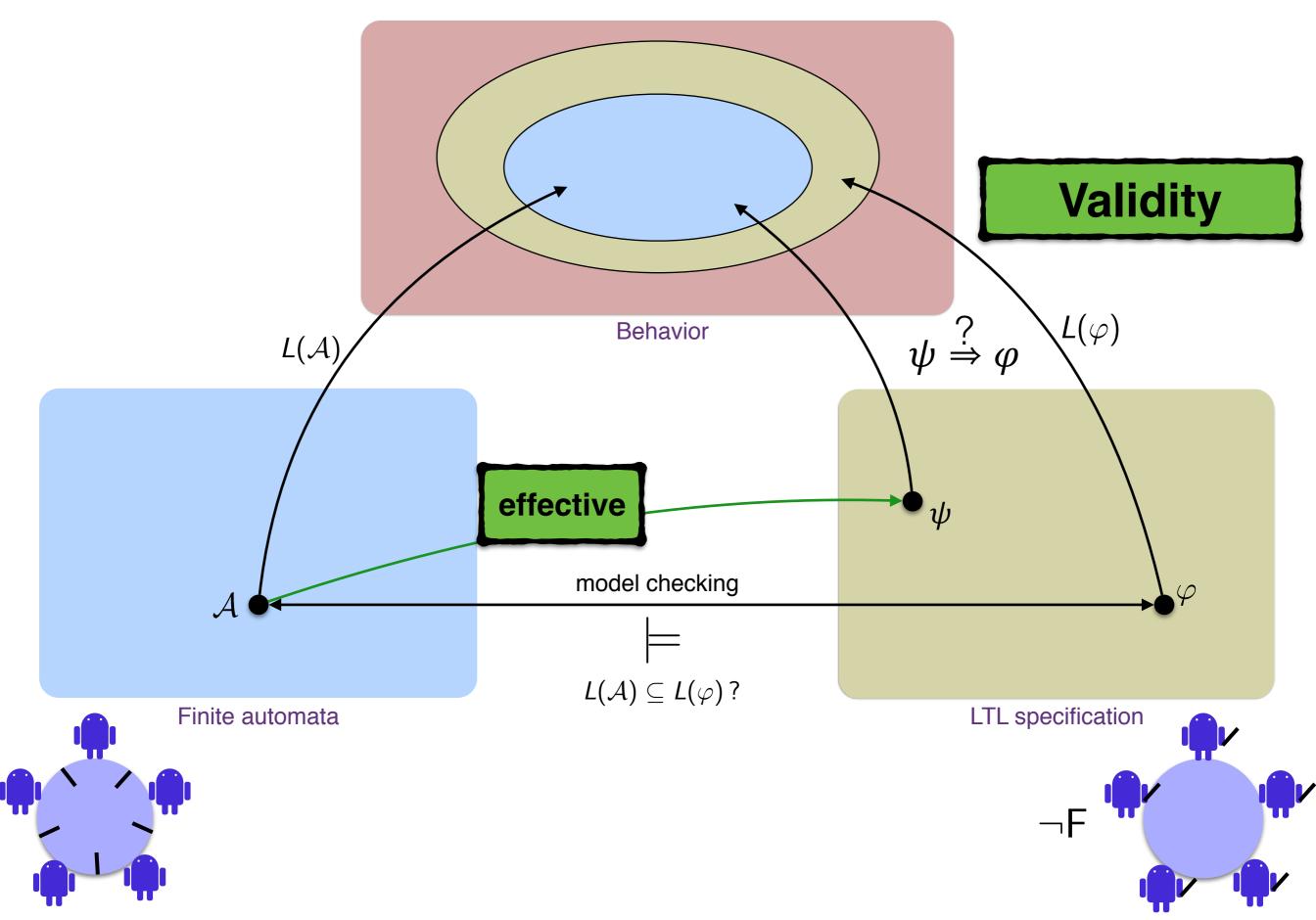
Joint work with C. Aiswarya & Benedikt Bollig CONCUR'15

DRV, Bertinoro, May 18, 2016

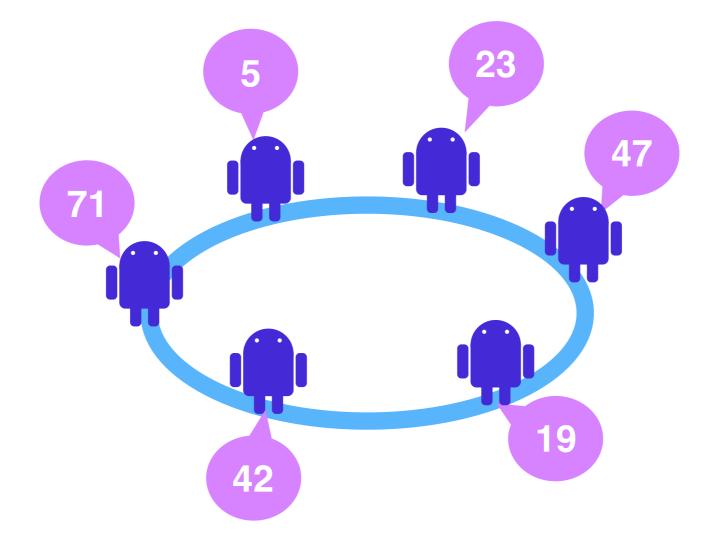


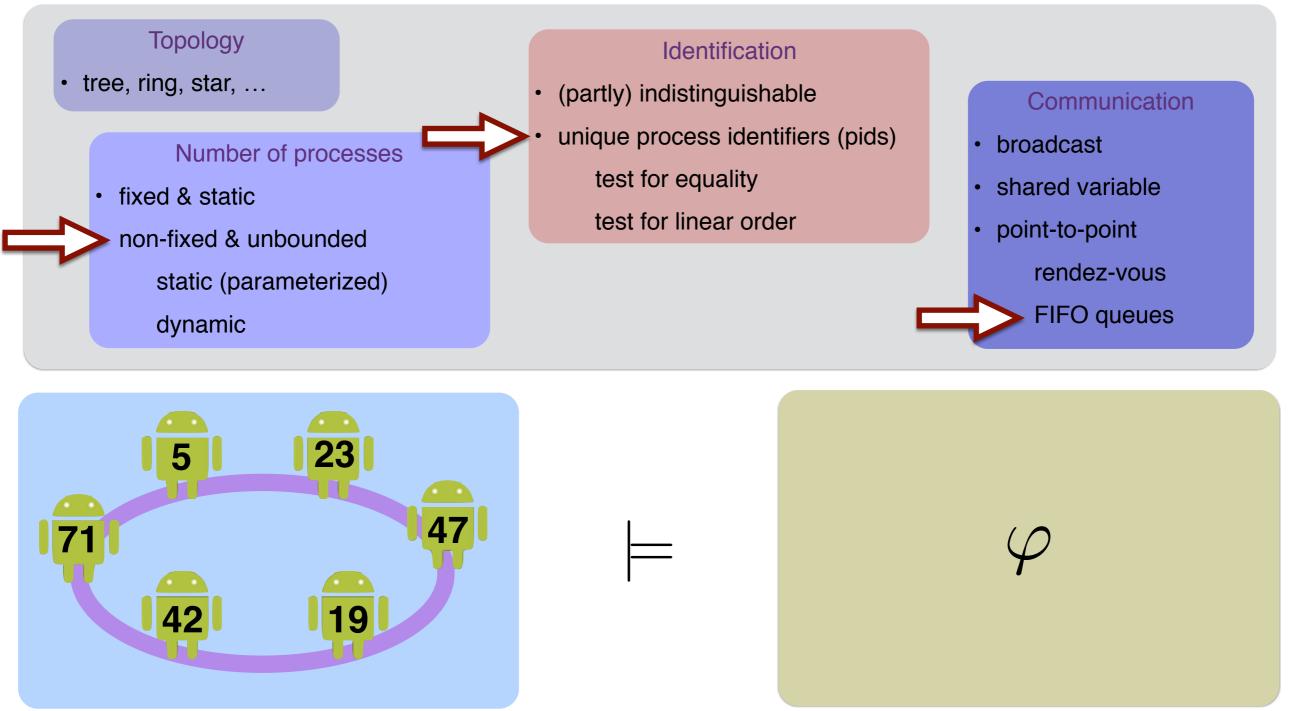






# Models of Distributed Systems

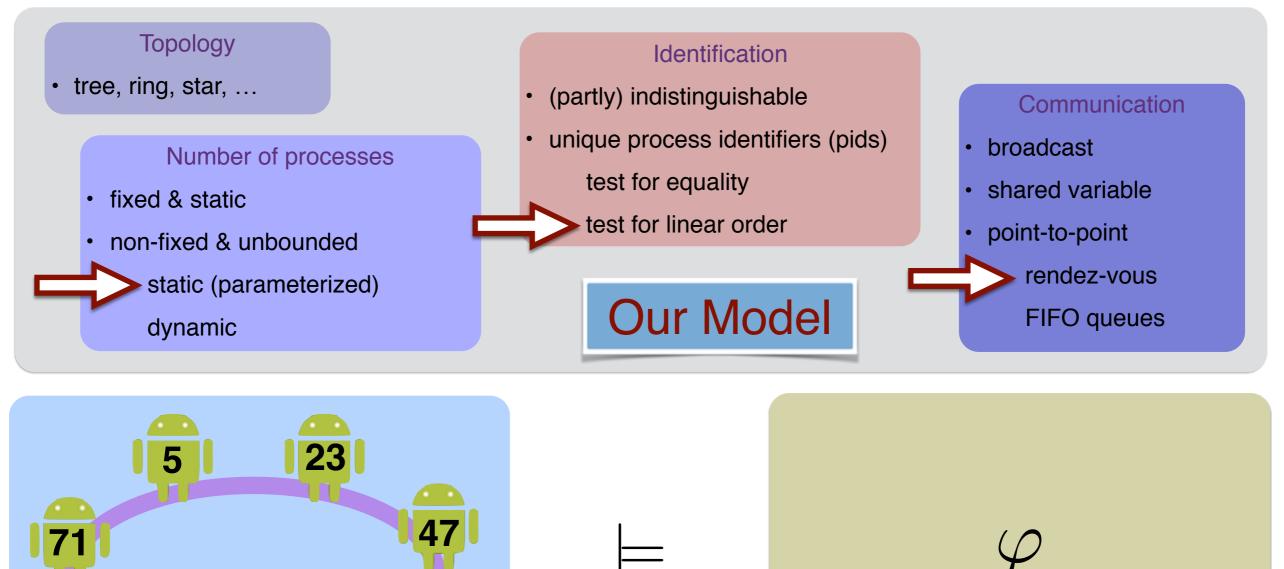




System model

Specification

# Several sources of infinity / undecidability



System model

Specification

# Several sources of infinity / undecidability

#### Leader election [Franklin '82]

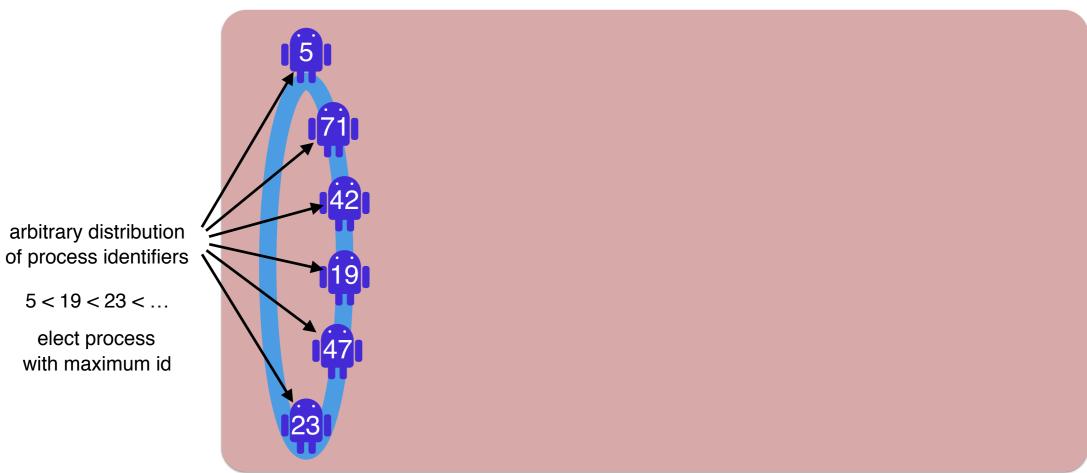
# **Distributed algorithms**

arbitrary number of identical processes



**Behavior** 

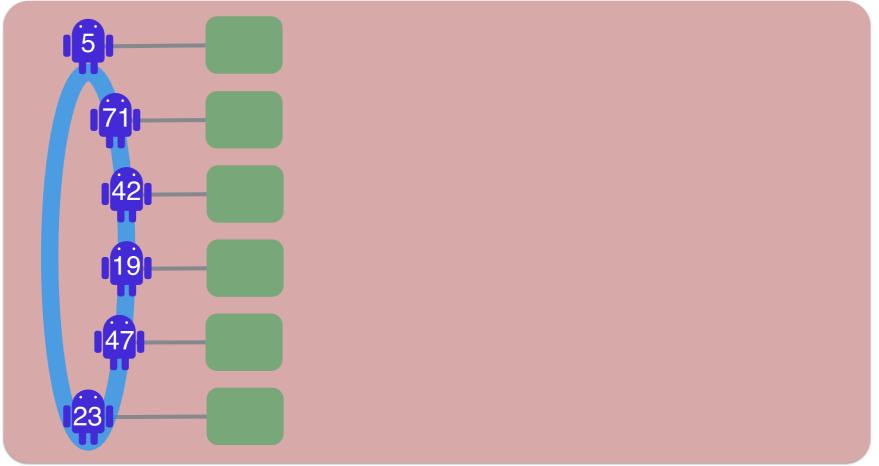




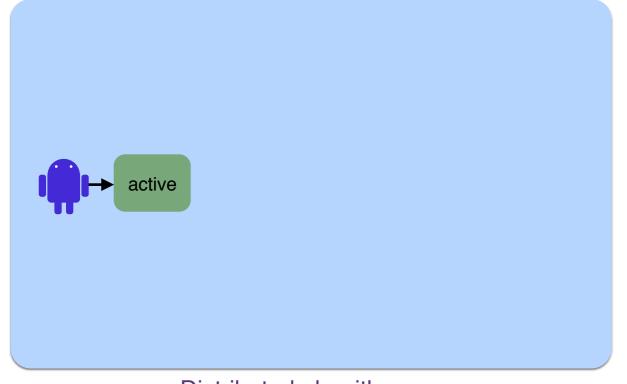
**Behavior** 

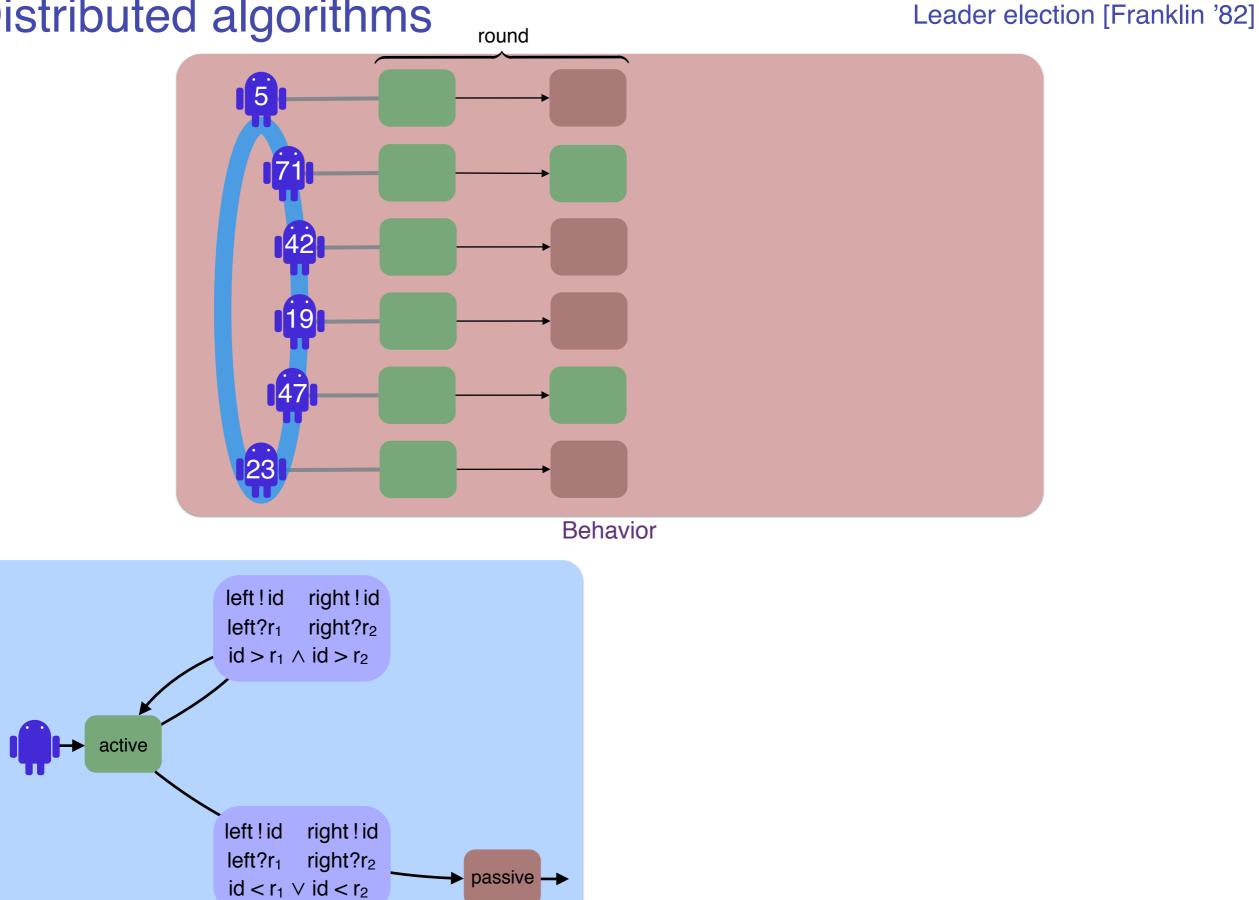




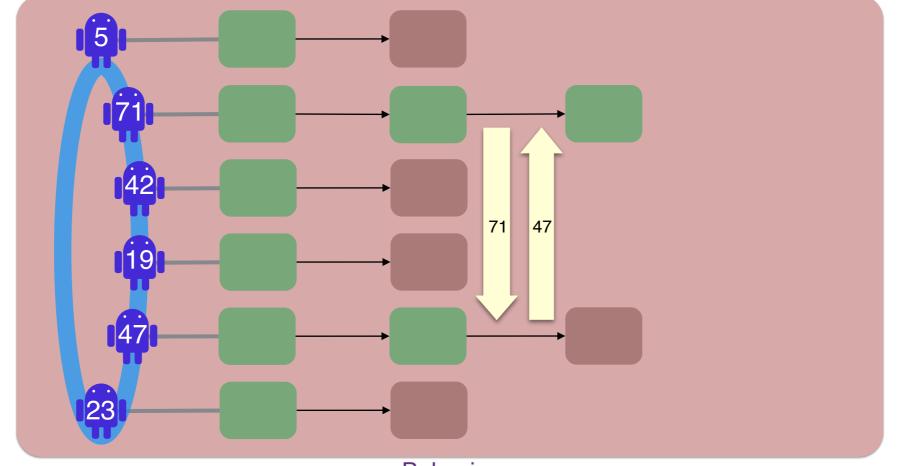


Behavior

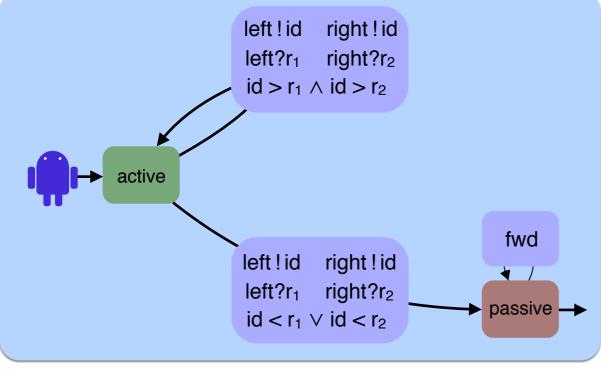


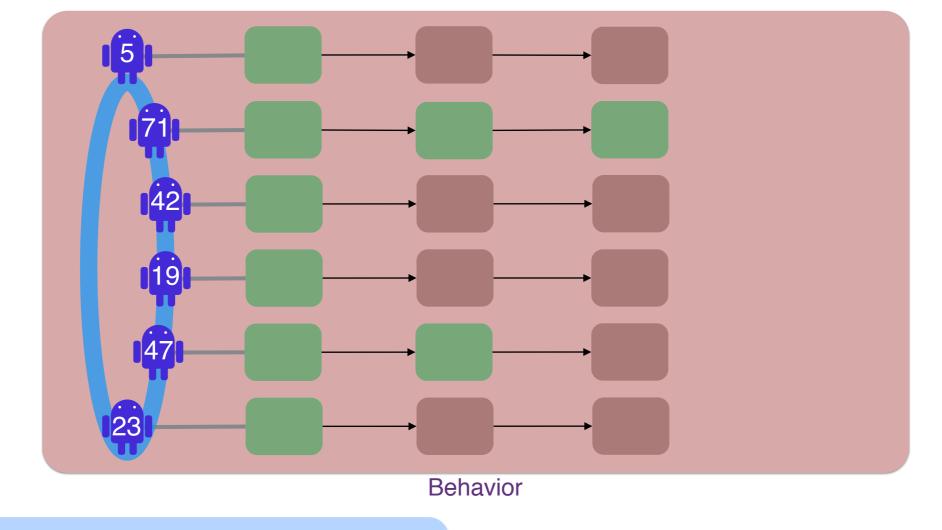


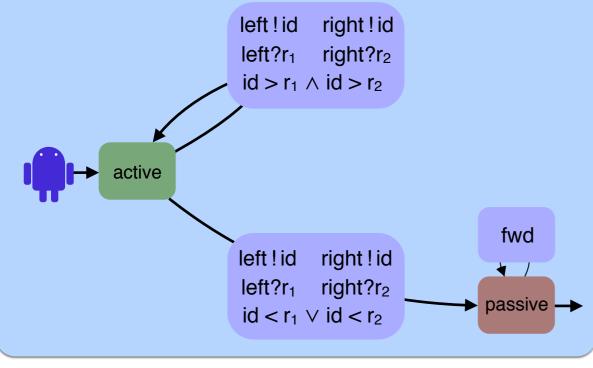
Leader election [Franklin '82]



**Behavior** 

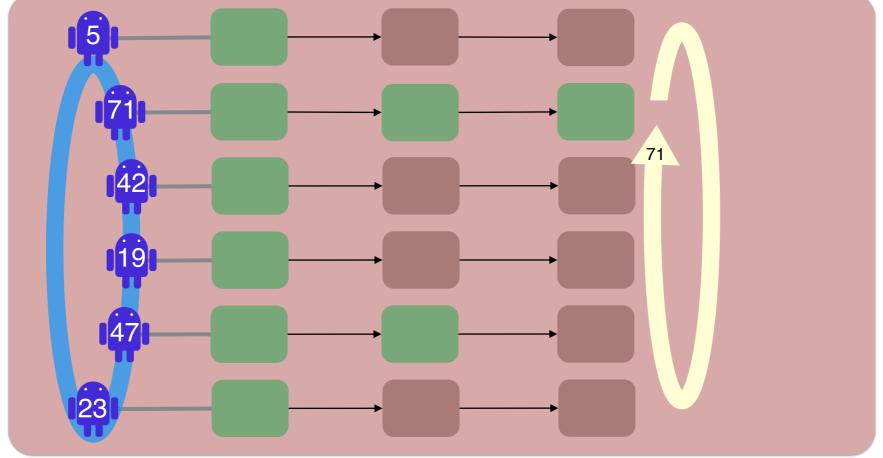




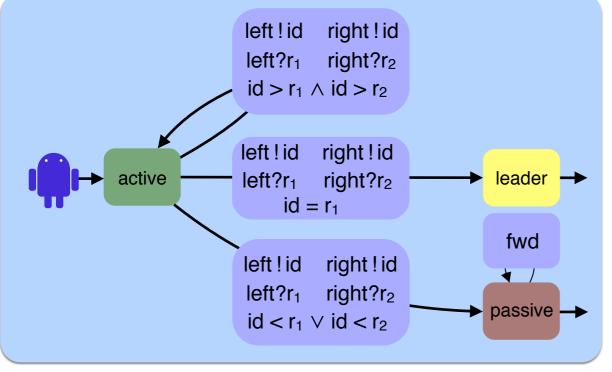


#### Leader election [Franklin '82]

# **Distributed algorithms**

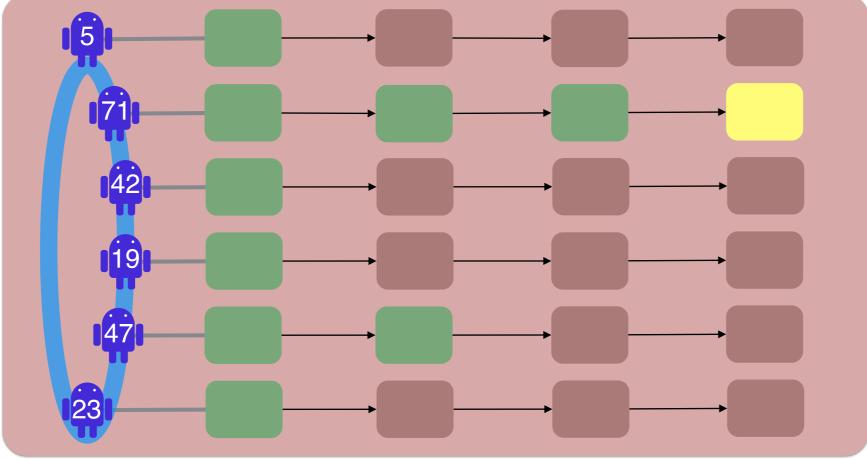


**Behavior** 

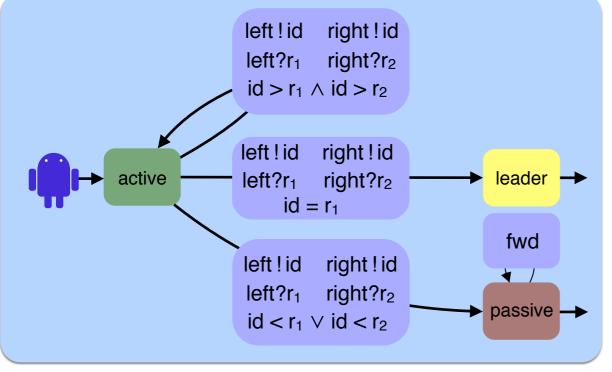


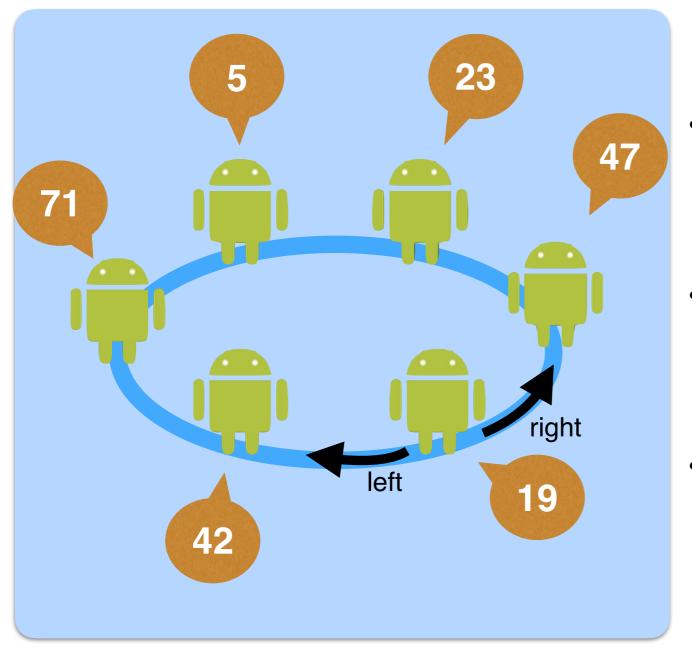
#### Leader election [Franklin '82]

# **Distributed algorithms**



**Behavior** 





- Identical finite-state processes
- Number of processes is unknown and unbounded
- Processes have unique pids (integers unbounded data)

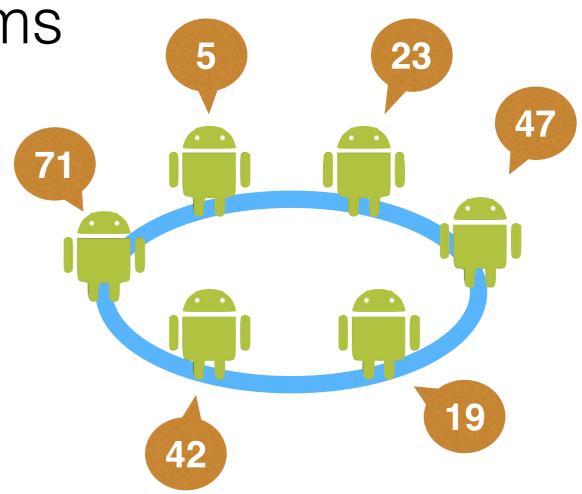
# A formal model for distributed algorithms An automata-like way of writing DA

Every process 📫 can be described by:

- Set of states
- Initial state
- Set of registers
  - stores pid

- Set of transitions
  - send pids to neighbours
  - receive pids from neighbours, and store in registers
  - compare registers
  - update registers

# Leader Election Algorithms Dolev-Klawe-Rhodeh82



$$t_{1} = \langle active_{0}: \mathbf{right}!r; \mathbf{left}?r'; \mathbf{goto} \ active_{1} \rangle$$
  

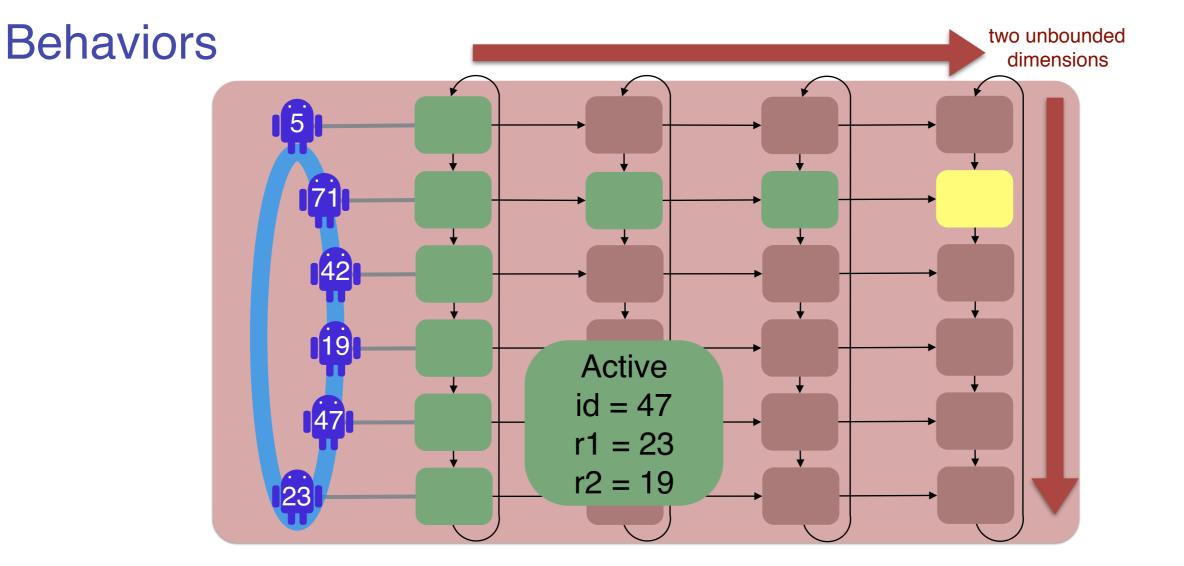
$$t_{2} = \langle active_{1}: \mathbf{right}!r'; \mathbf{left}?r''; r'' < r'; r < r'; r := r'; \mathbf{goto} \ active_{0} \rangle$$
  

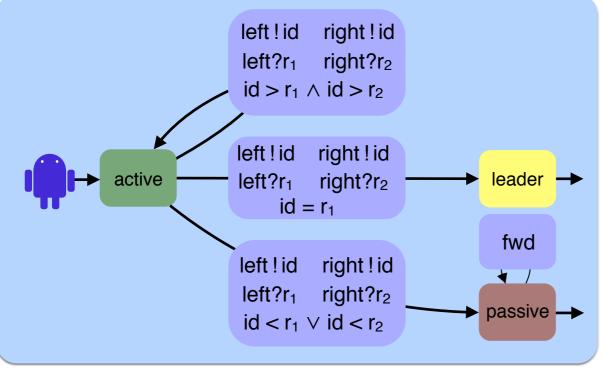
$$t_{3} = \langle active_{1}: \_ ; r' < r; \mathbf{goto} \ passive \rangle$$
  

$$t_{4} = \langle active_{1}: \_ ; r' < r''; \mathbf{goto} \ passive \rangle$$
  

$$t_{5} = \langle active_{1}: \_ ; r = r'; \mathbf{goto} \ found \rangle$$
  

$$t_{6} = \langle passive: \mathbf{fwd}; \mathbf{left}?r; \mathbf{goto} \ passive \rangle$$

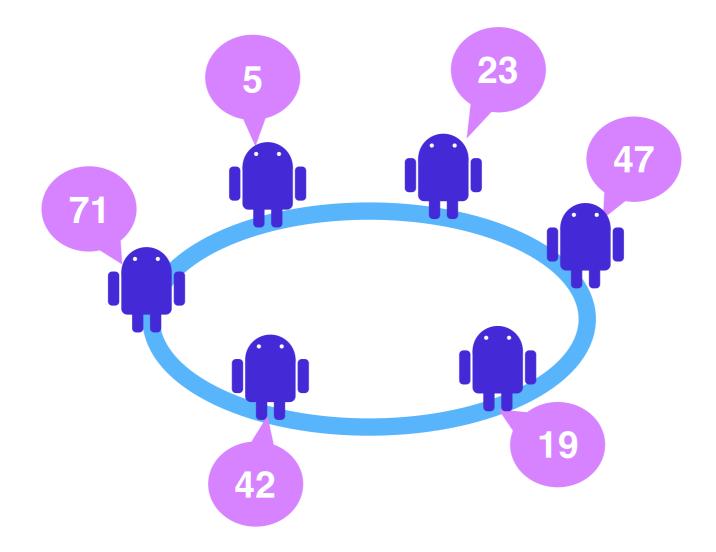




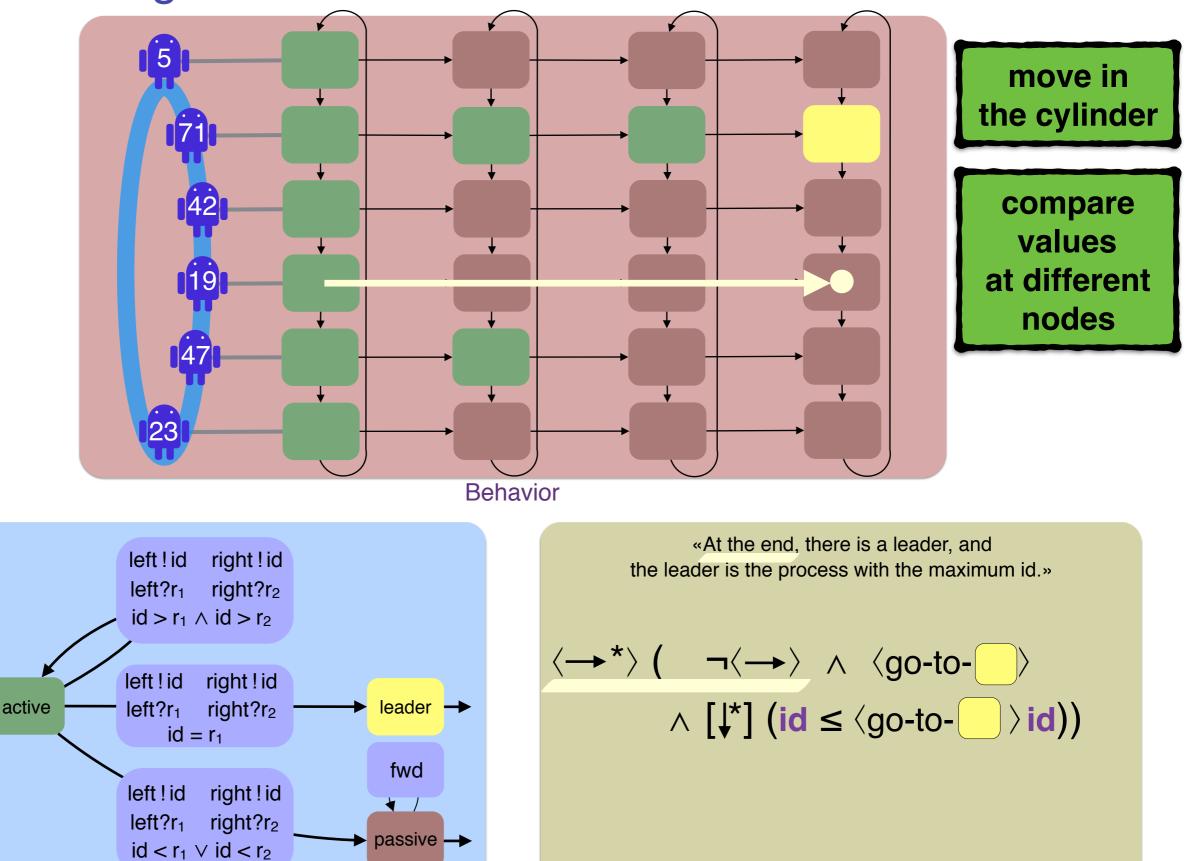
Cylinders Arbitrary length and width Labelled with data from an infinite domain

# **3 sources of infinity**

# Specification language



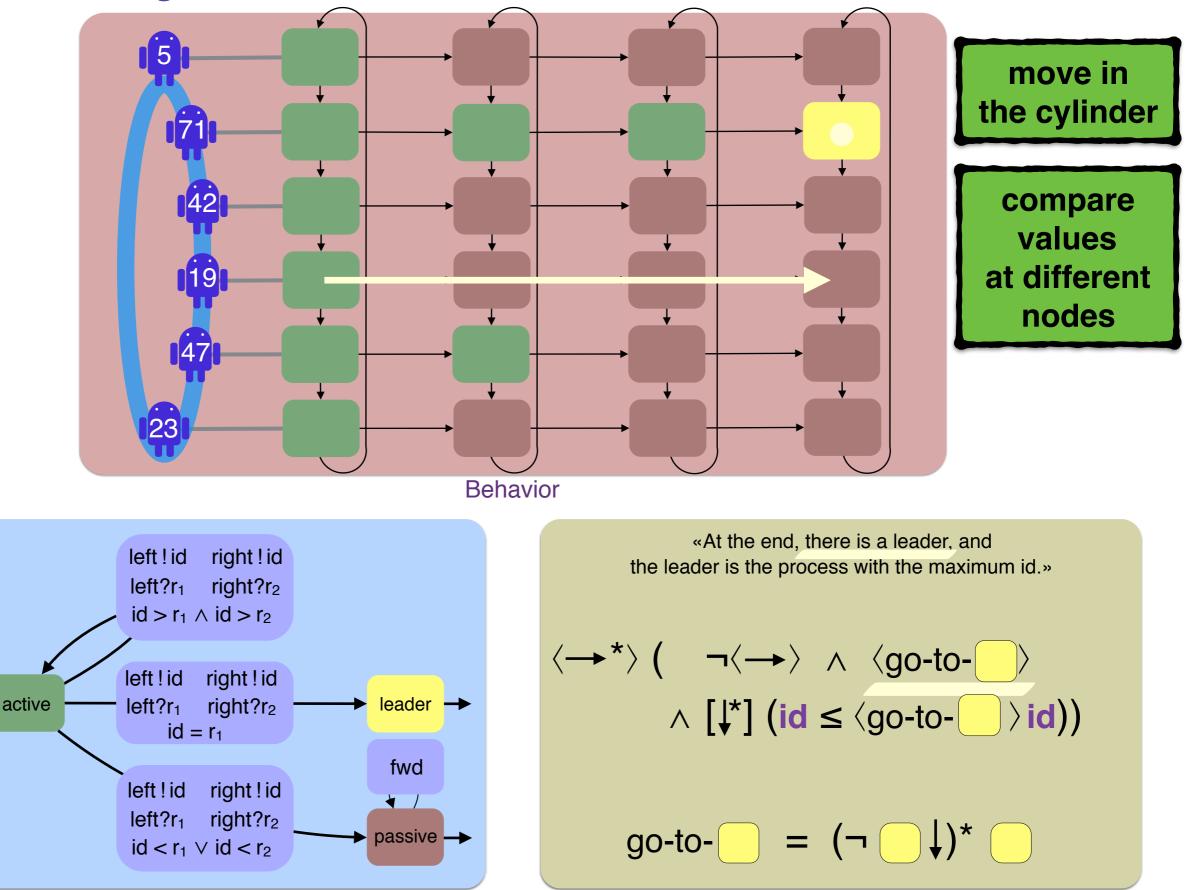
Leader election [Franklin '82]



Distributed algorithm

Data Propositional Dynamic Logic [Bojanczyk et al. '09; Figueira-Segoufin '11]

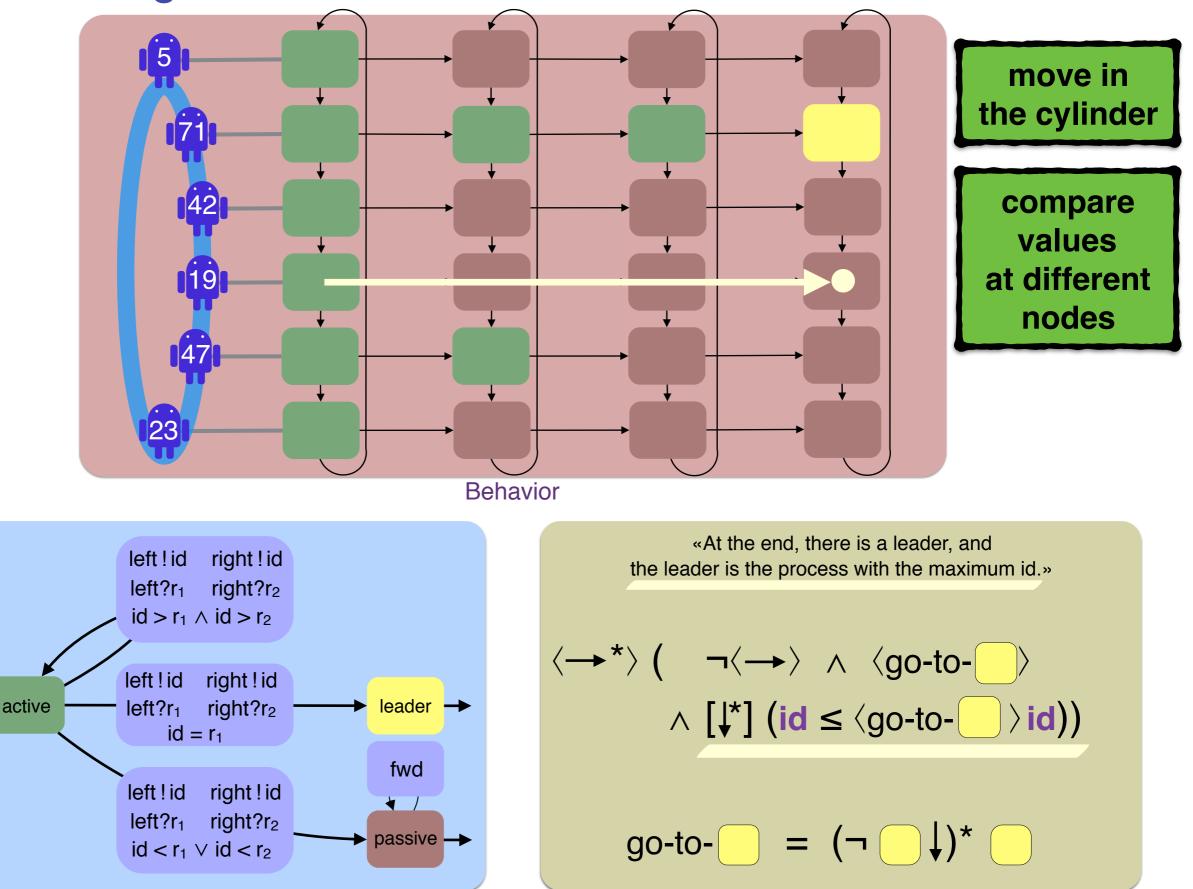
Leader election [Franklin '82]



Distributed algorithm

Data Propositional Dynamic Logic [Bojanczyk et al. '09; Figueira-Segoufin '11]

Leader election [Franklin '82]

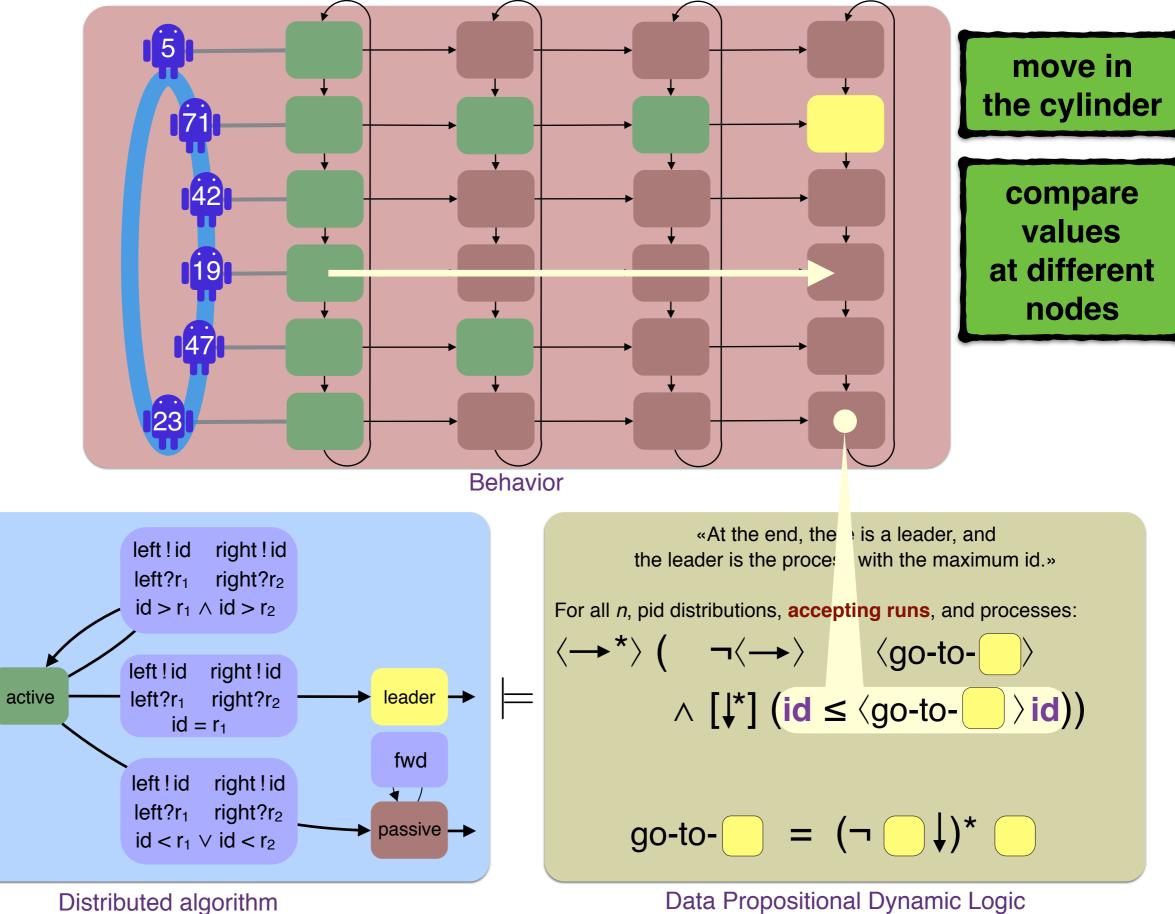


Distributed algorithm

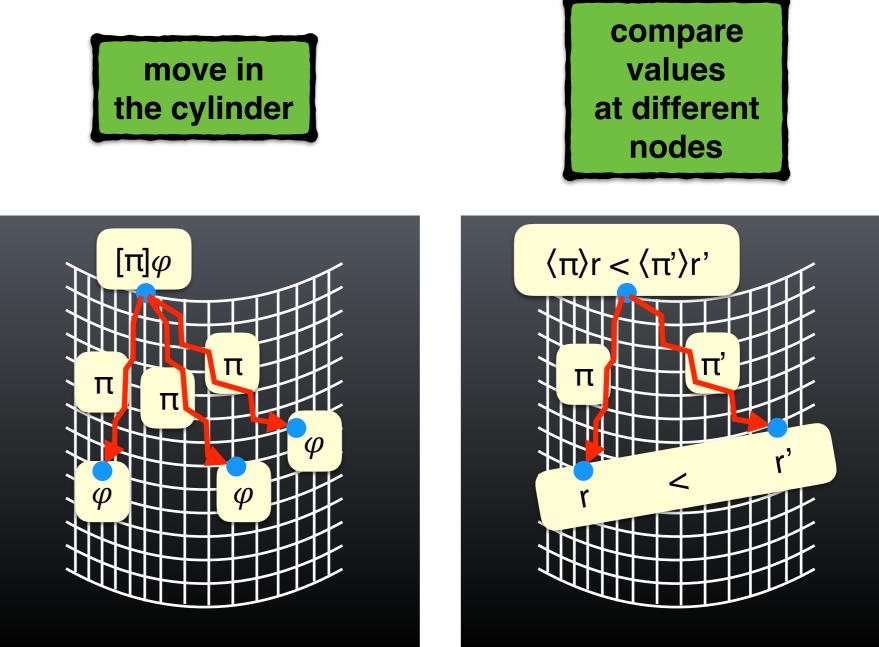
Data Propositional Dynamic Logic [Bojanczyk et al. '09; Figueira-Segoufin '11]

Leader election [Franklin '82]

[Bojanczyk et al. '09; Figueira-Segoufin '11]



# Specifications Data PDL

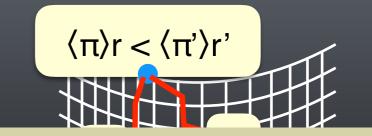


Path  $\pi$  = rational expression over directions

Inspired by [Bojanczyk et al. '09; Figueira-Segoufin '11]







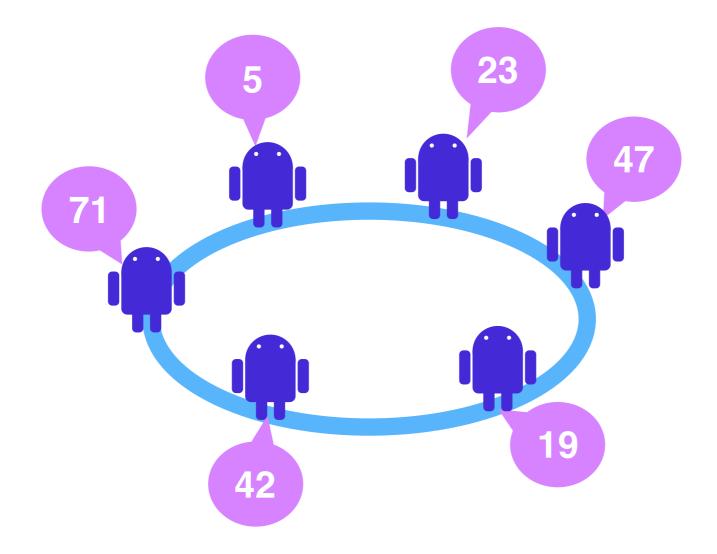
For rings of all sizes, all pid distributions, all accepting runs, and all starting process (m)  $\varphi, \varphi' ::= \mathsf{m} \mid s \mid \neg \varphi \mid \varphi \land \varphi' \mid \varphi \Rightarrow \varphi' \mid [\pi]\varphi \mid \langle \pi \rangle r \bowtie \langle \pi' \rangle r'$  $\pi, \pi' ::= \{\varphi\}? \mid d \mid \pi + \pi' \mid \pi \cdot \pi' \mid \pi^*$ 

 $s \in S, r, r' \in Reg, \bowtie \in \{=, \neq, <, \leq\}, \text{ and } d \in \{\epsilon, \leftarrow, \rightarrow, \uparrow, \downarrow\}$ 

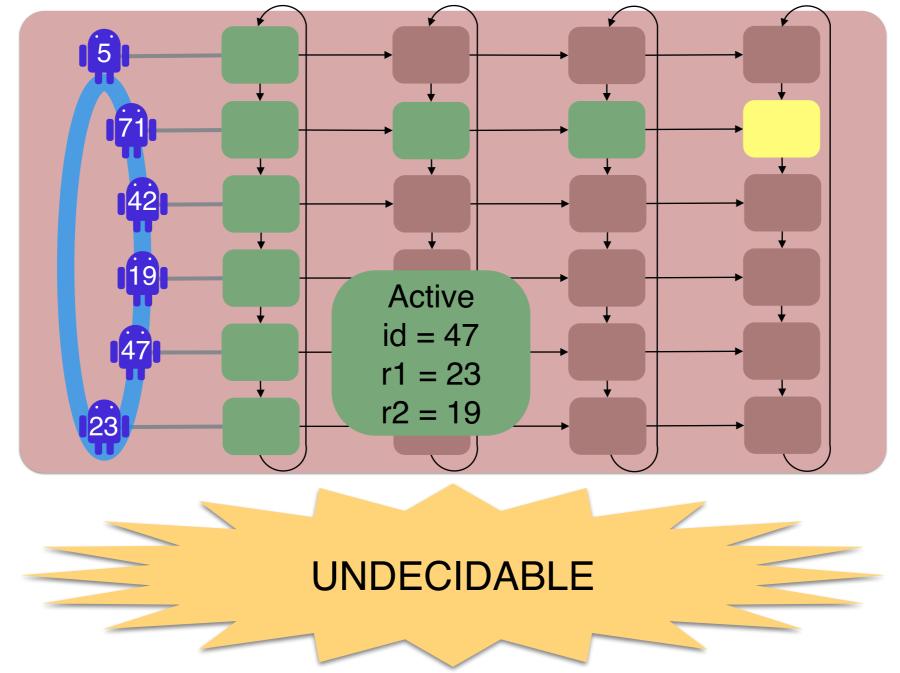
#### Path $\pi$ = rational expression over directions

Inspired by [Bojanczyk et al. '09; Figueira-Segoufin '11]

# Model Checking 1

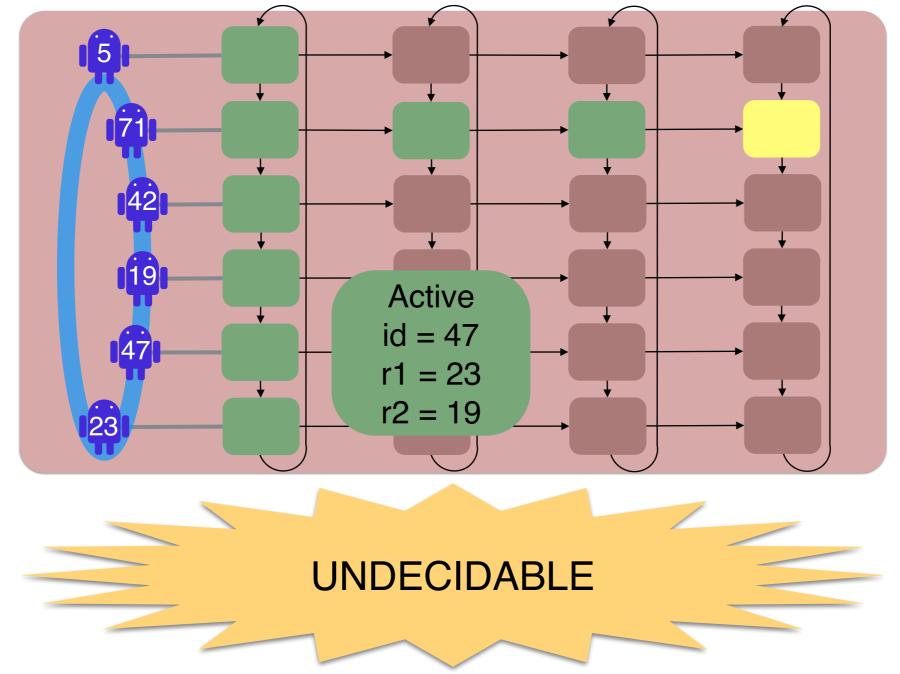


# Model Checking Distributed algorithms



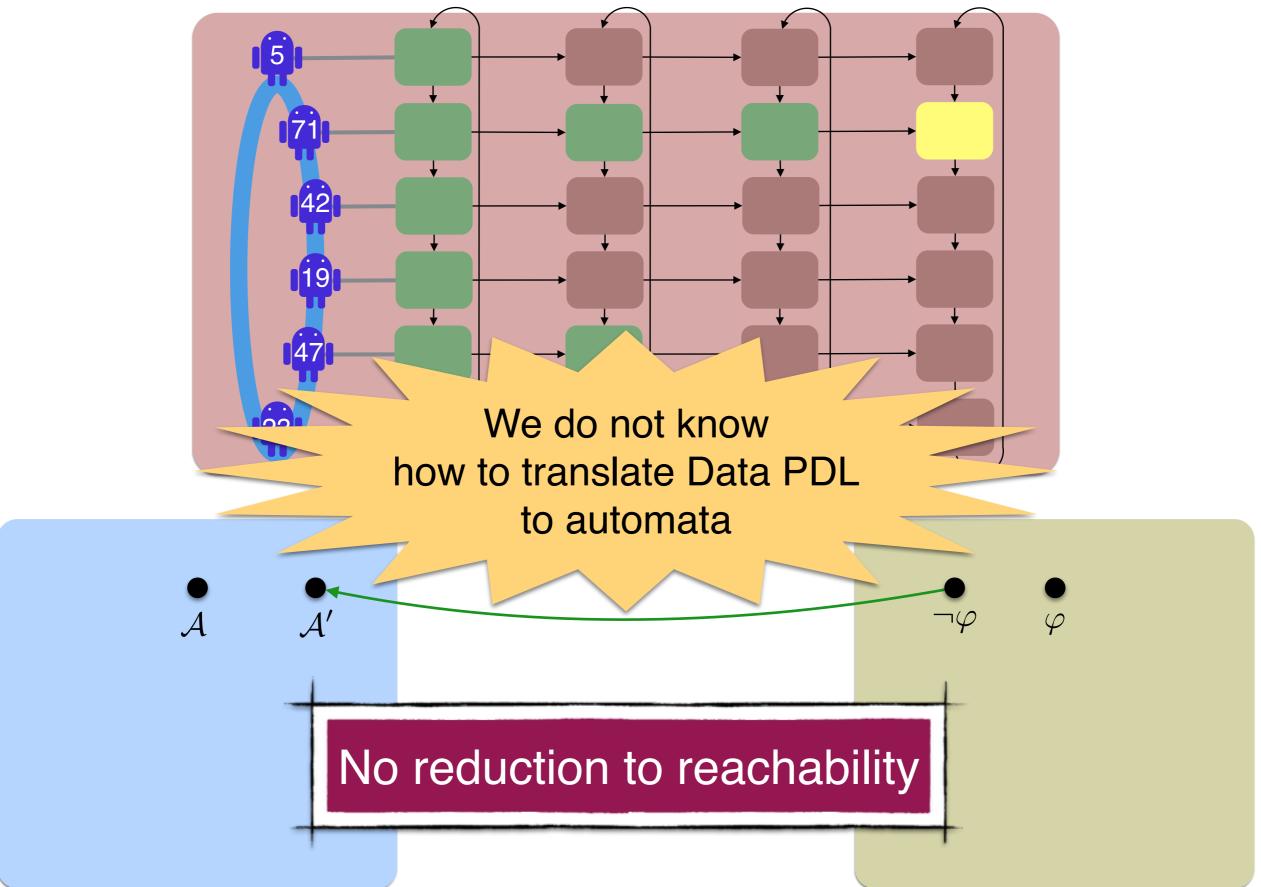
- Behaviors: Cylinders of arbitrary width and length Data from an infinite domain
- System: Register automata with data comparisons
- Specification: Data PDL with data comparisons

# Model Checking Distributed algorithms



- Behaviors: Cylinders of arbitrary width and length
   Data from an infinite domain
- System: Register automata with data comparisons
- Specification: Data PDL with data comparisons

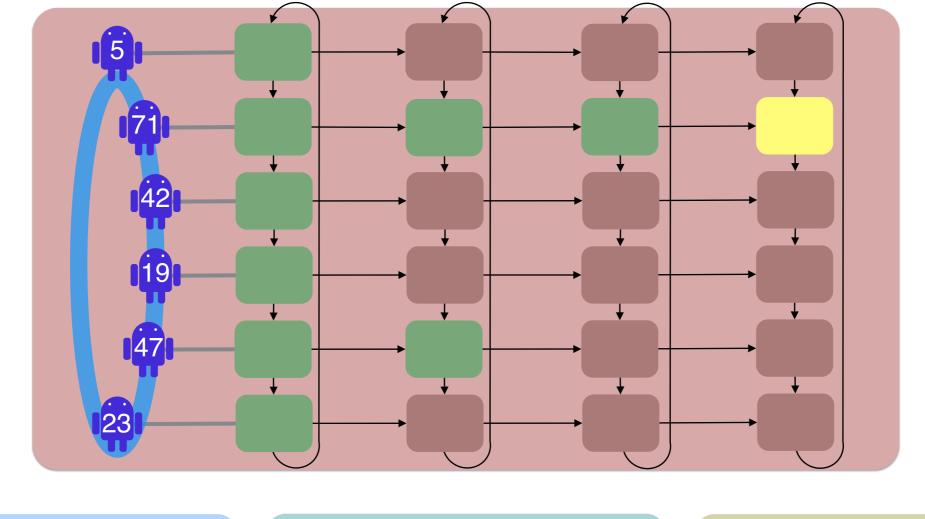
#### Reduction to automata?

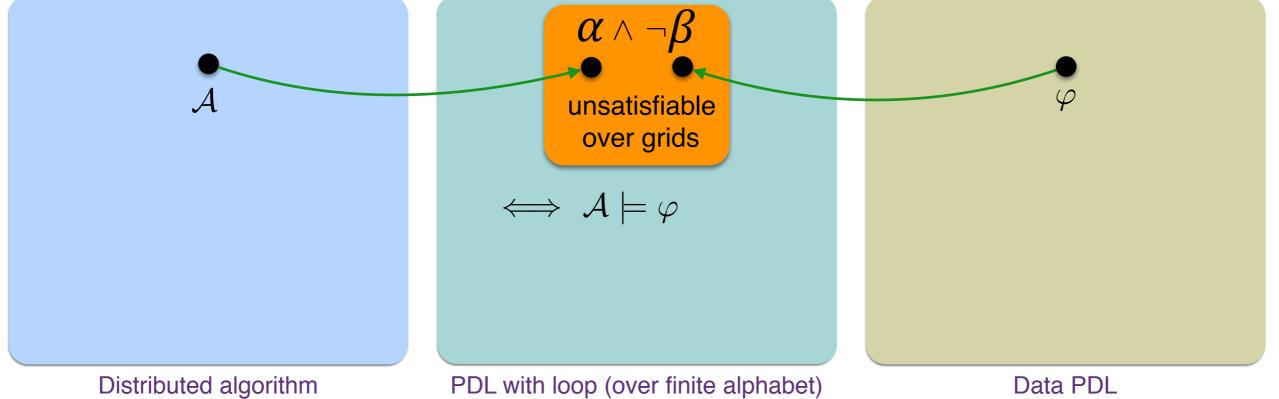


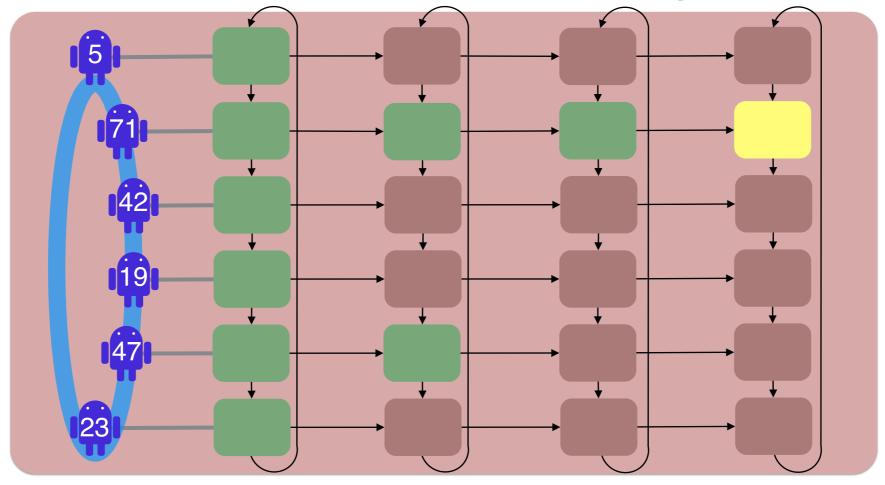
Distributed algorithm

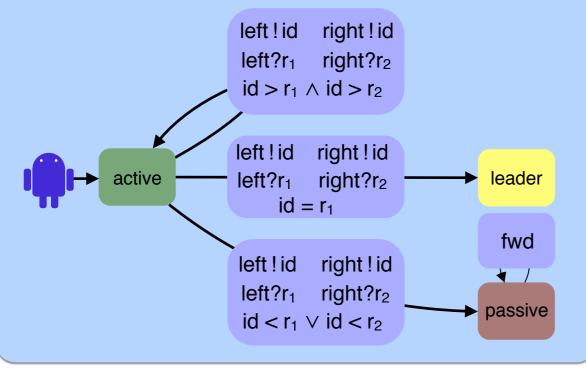
Data PDL

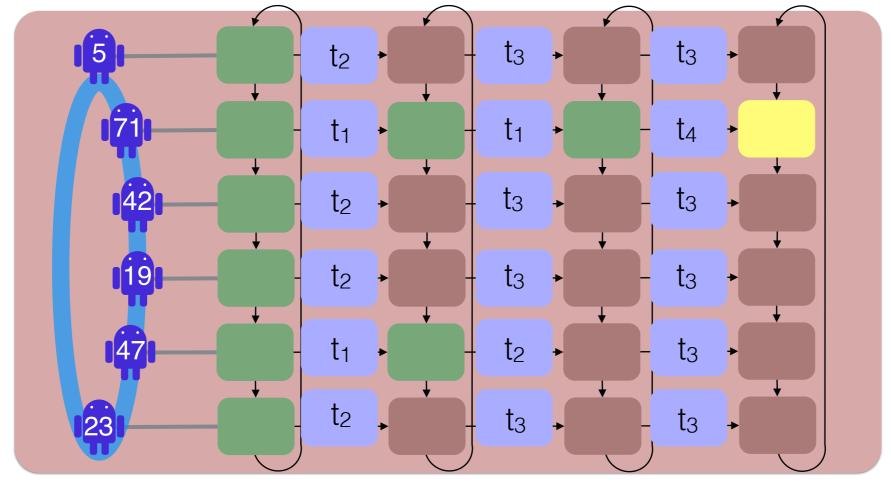
# Reduction to Satisfiability of LCPDL: Data abstraction

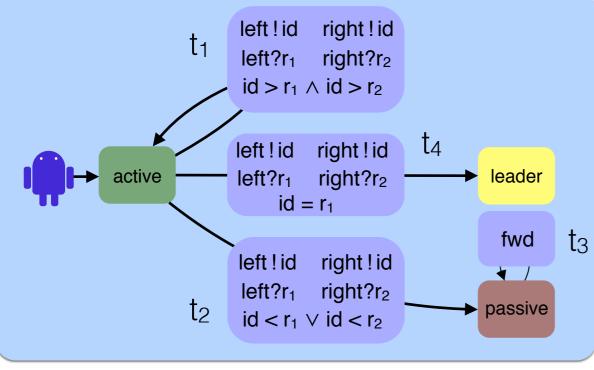


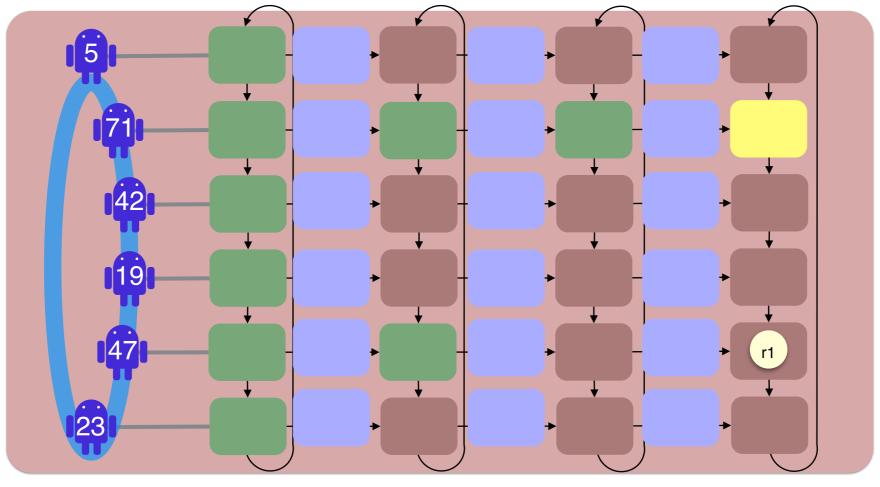




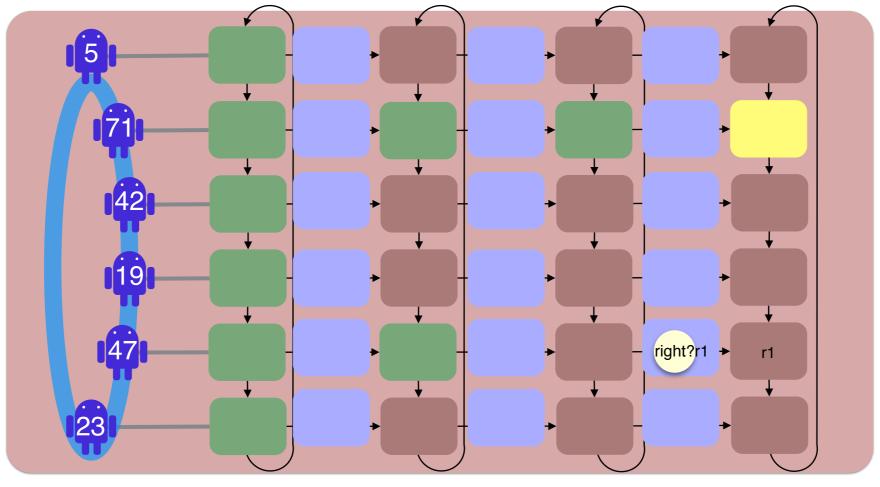




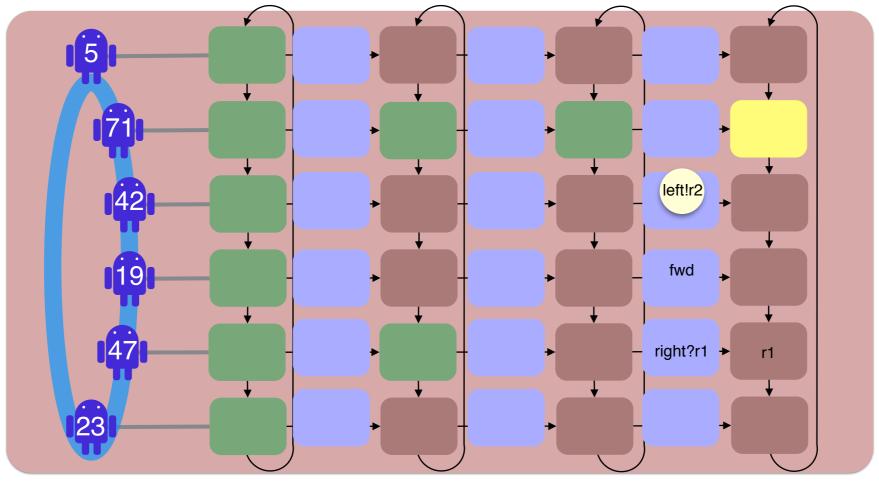




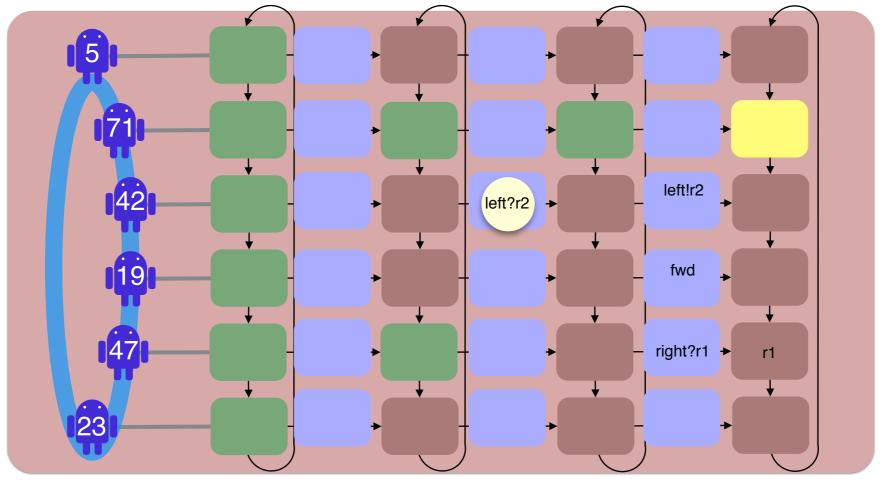
• Register updates



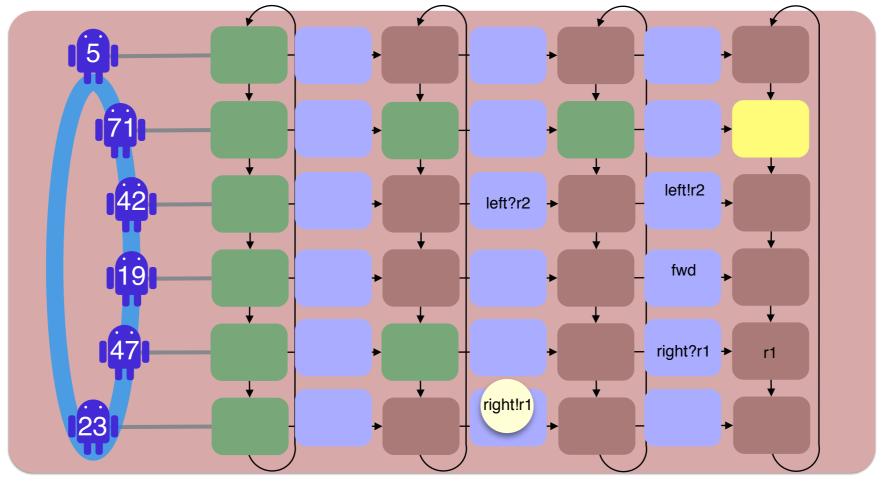
• Register updates



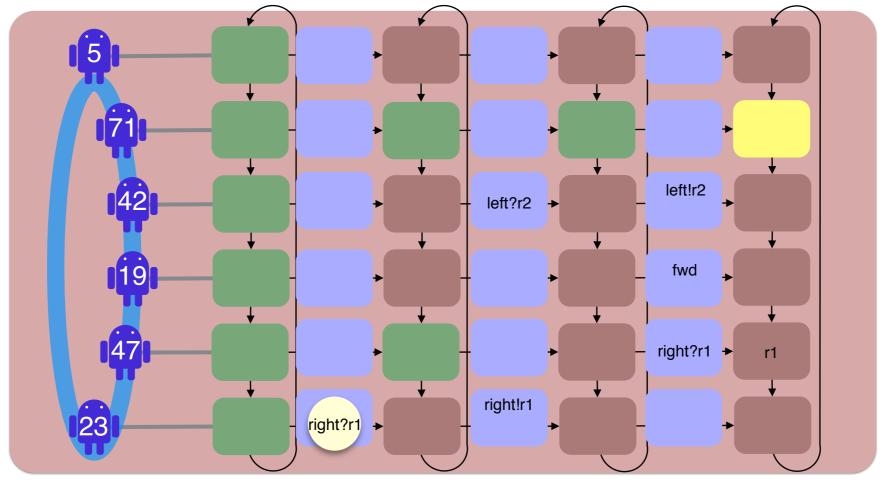
• Register updates



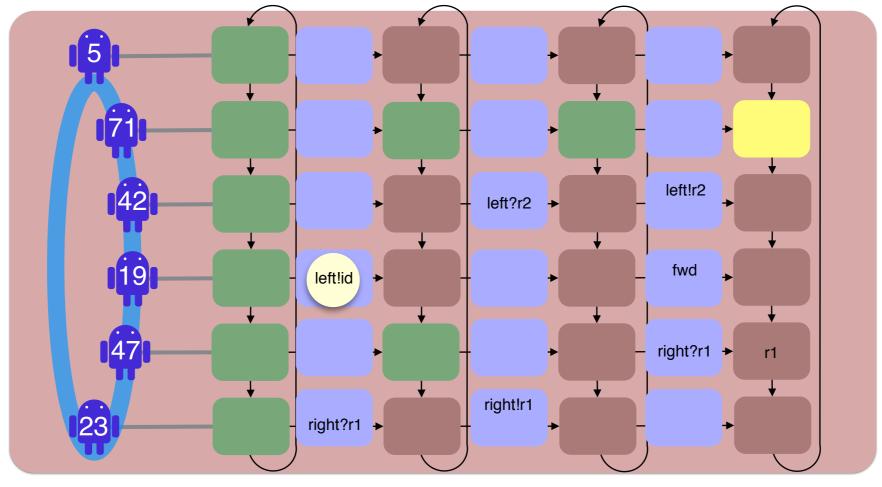
• Register updates



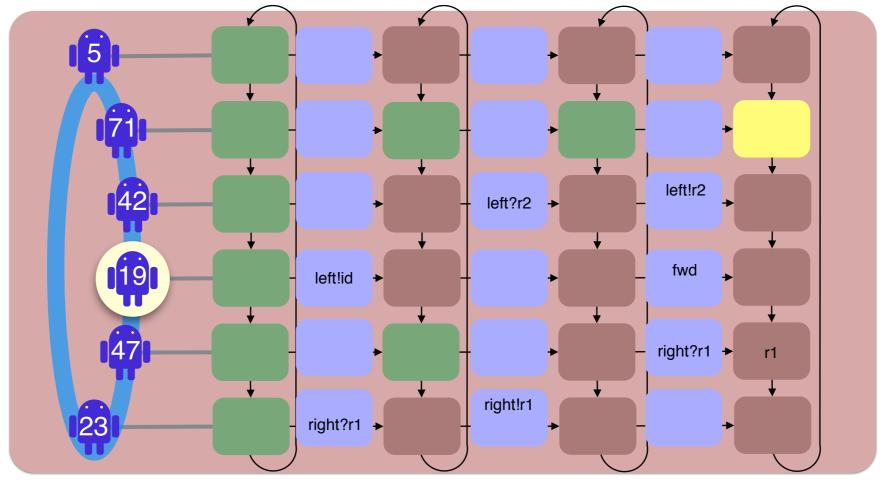
• Register updates



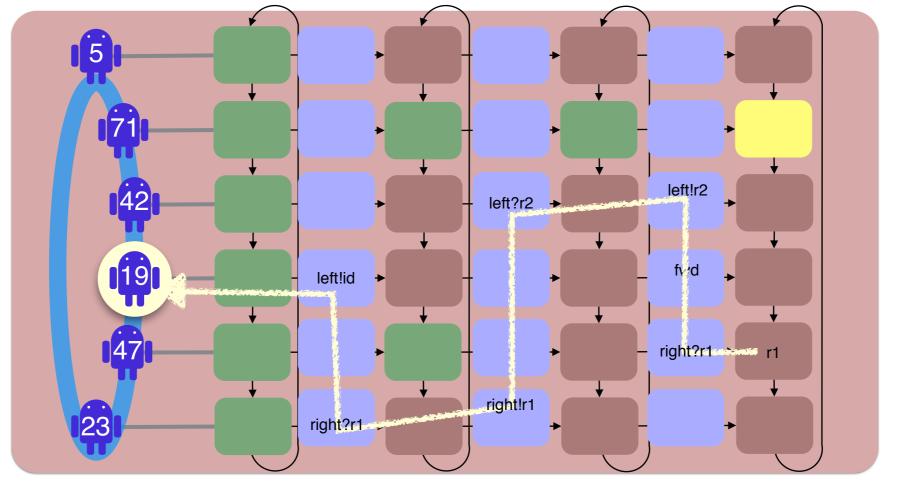
• Register updates



• Register updates



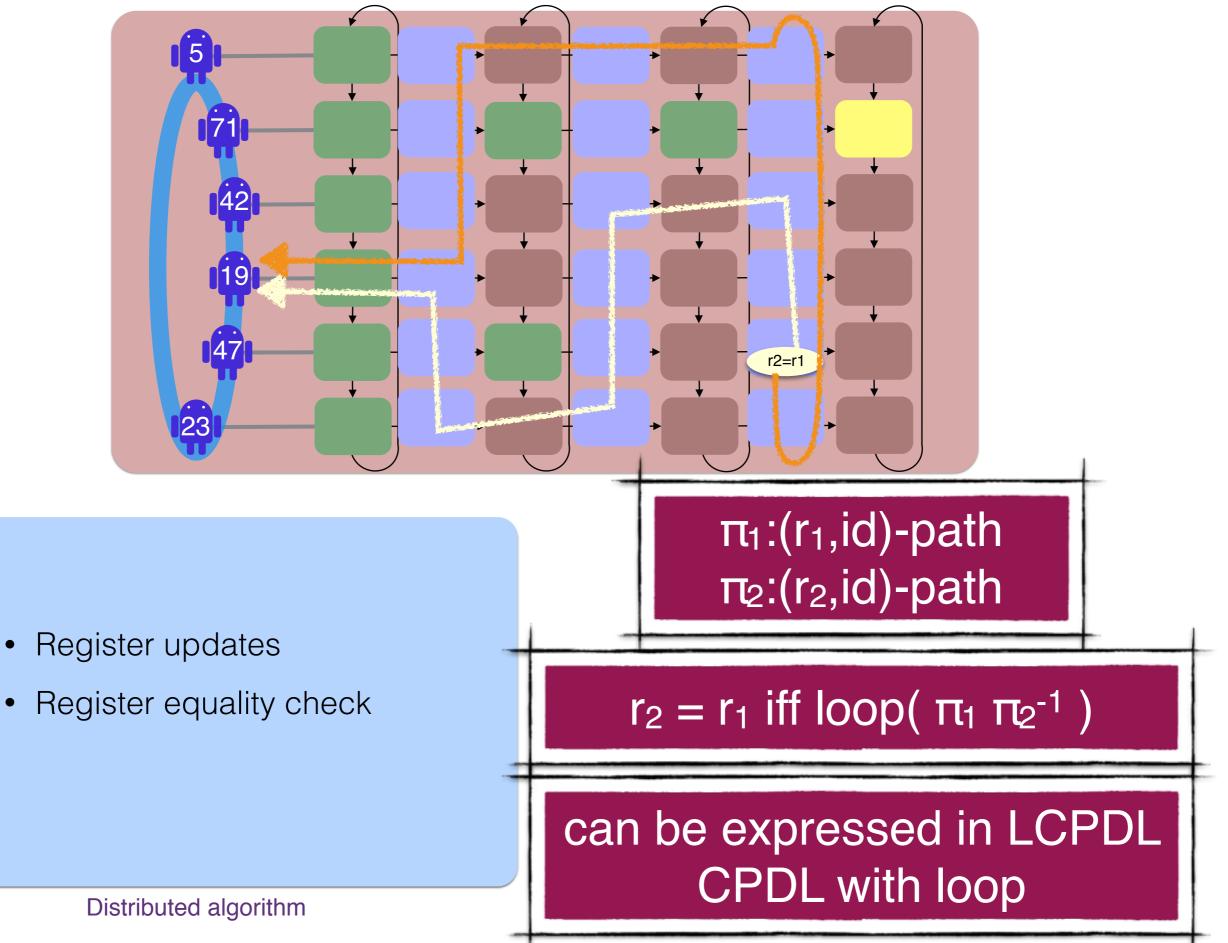
• Register updates

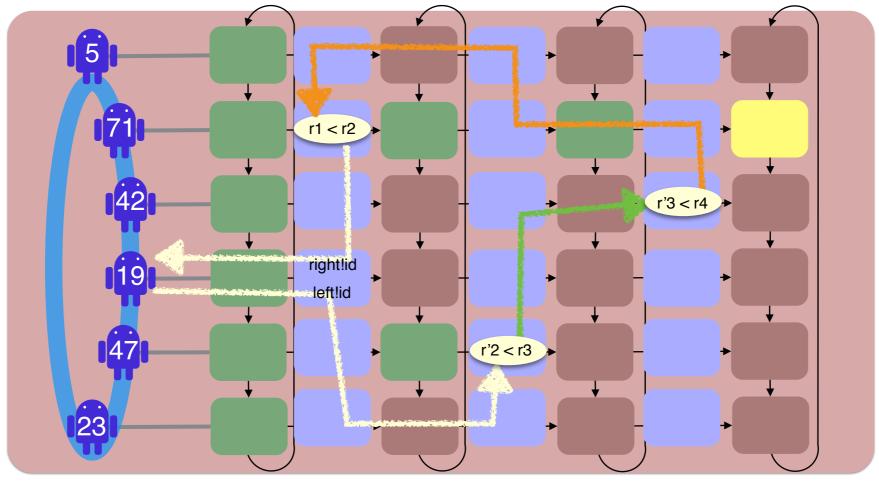


• Register updates

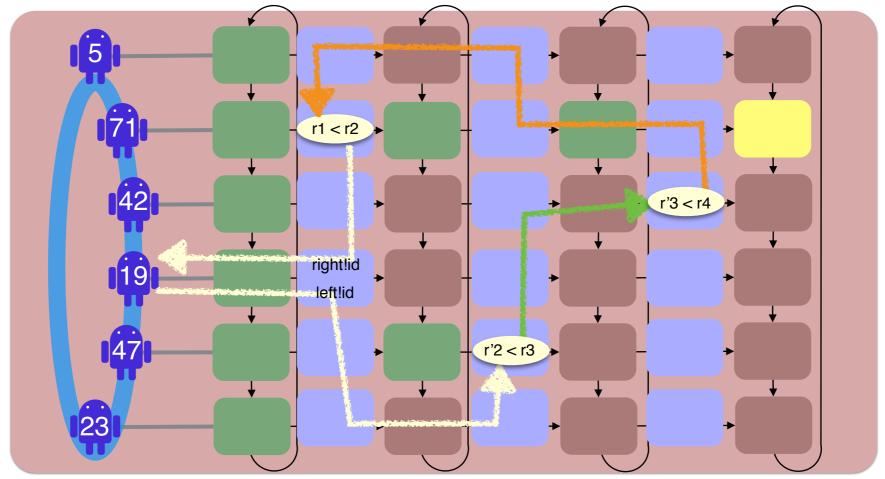
#### can be expressed in CPDL PDL with converse

(r<sub>1</sub>,id)-path

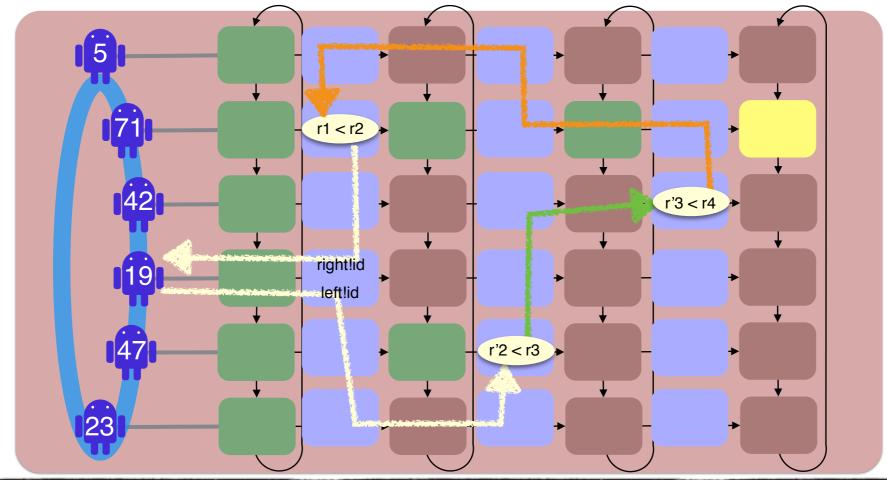




- Register updates
- Register equality check
- Register comparison



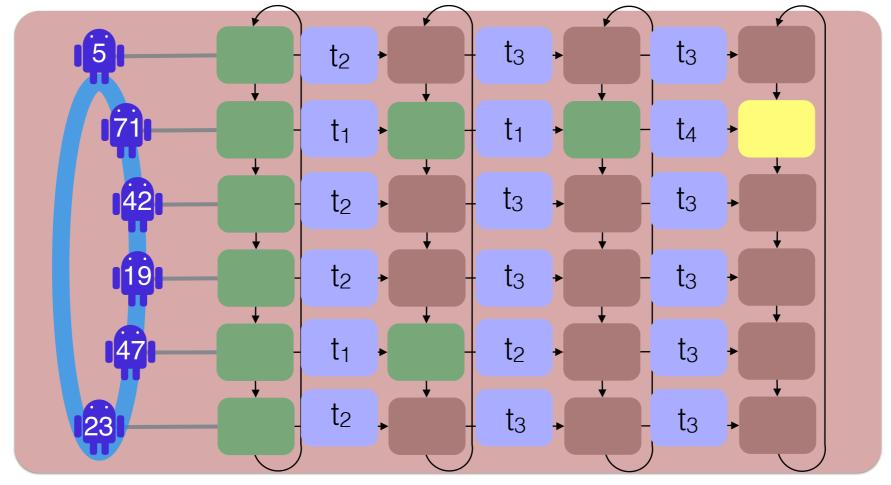
- If there is a <-loop, no pids assignments can turn the symbolic cylinder into a valid run.
- If no such loops, then there are pids that allow a valid realization of the abstract grid

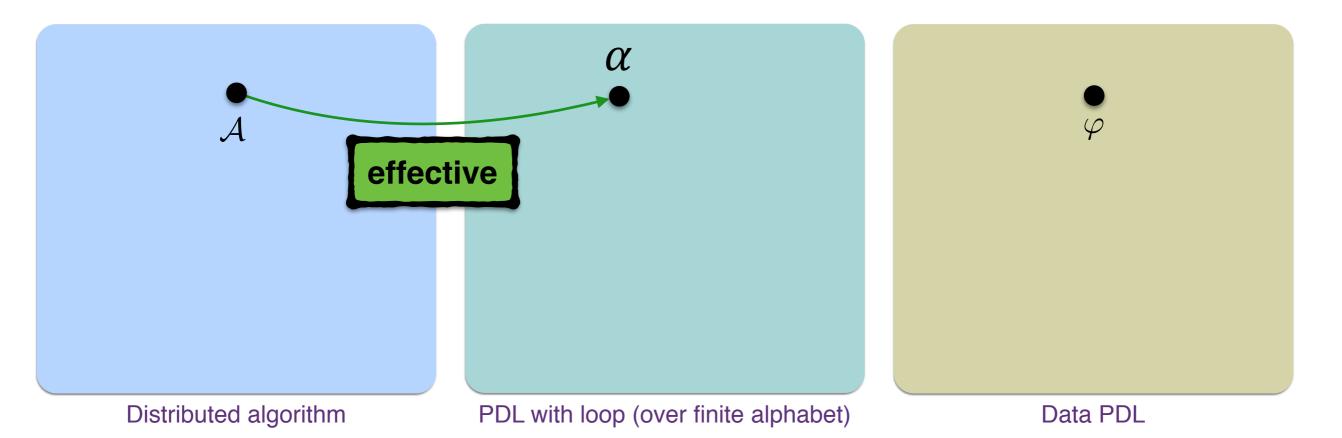


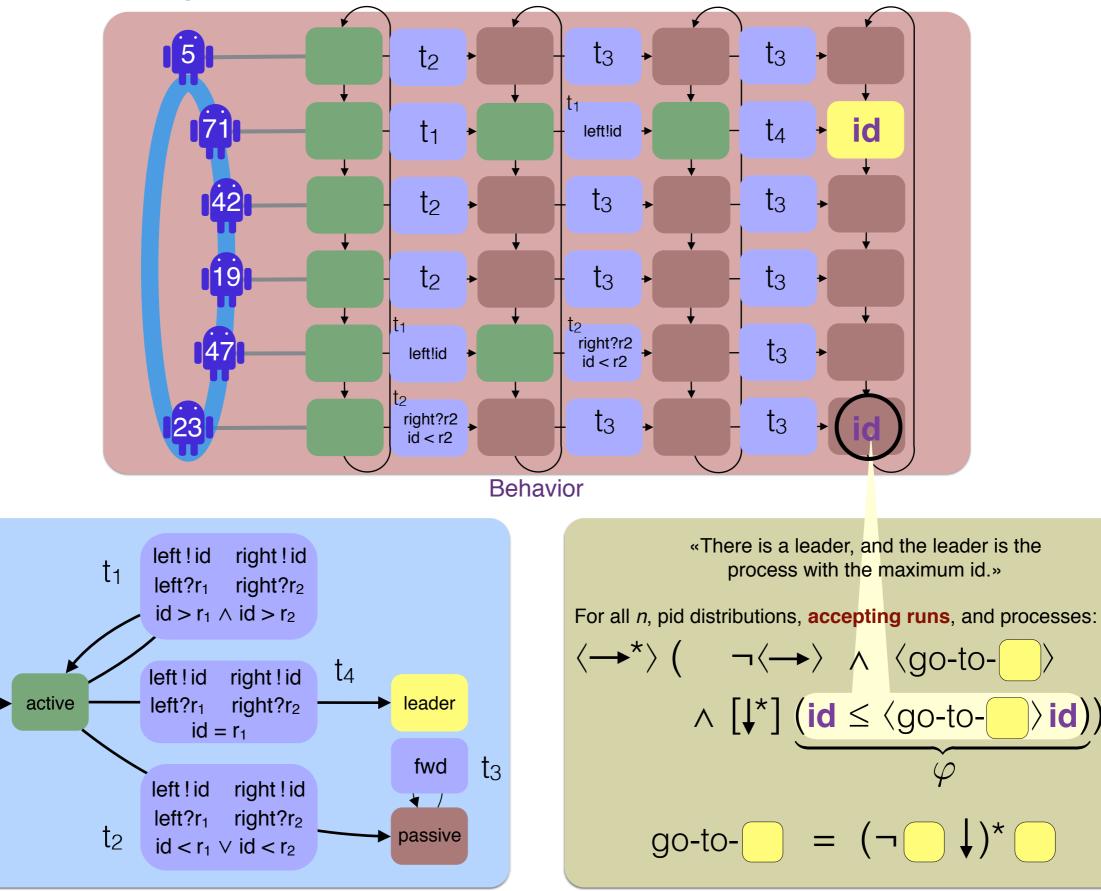
#### No loop of the form $r_{i0} < r_{i1}$ ; $(r_{i1}, r_{i2})$ -path; $r_{i2} < r_{i3}$ ; $(r_{i3}, r_{i4})$ -path; ...; $r_{in} < r_{i0}$

- Register updates
- Register equality check
- Register comparison

can be expressed in LCPDL CPDL with loop



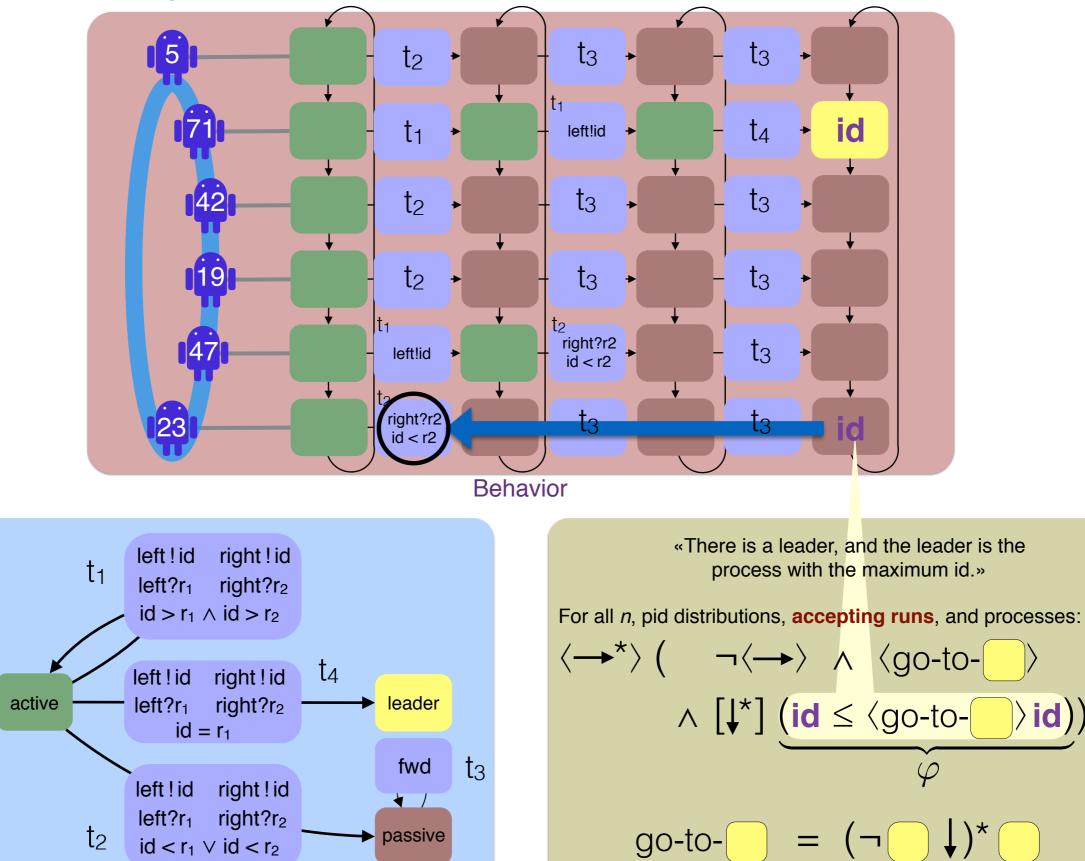




Distributed algorithm

Data PDL

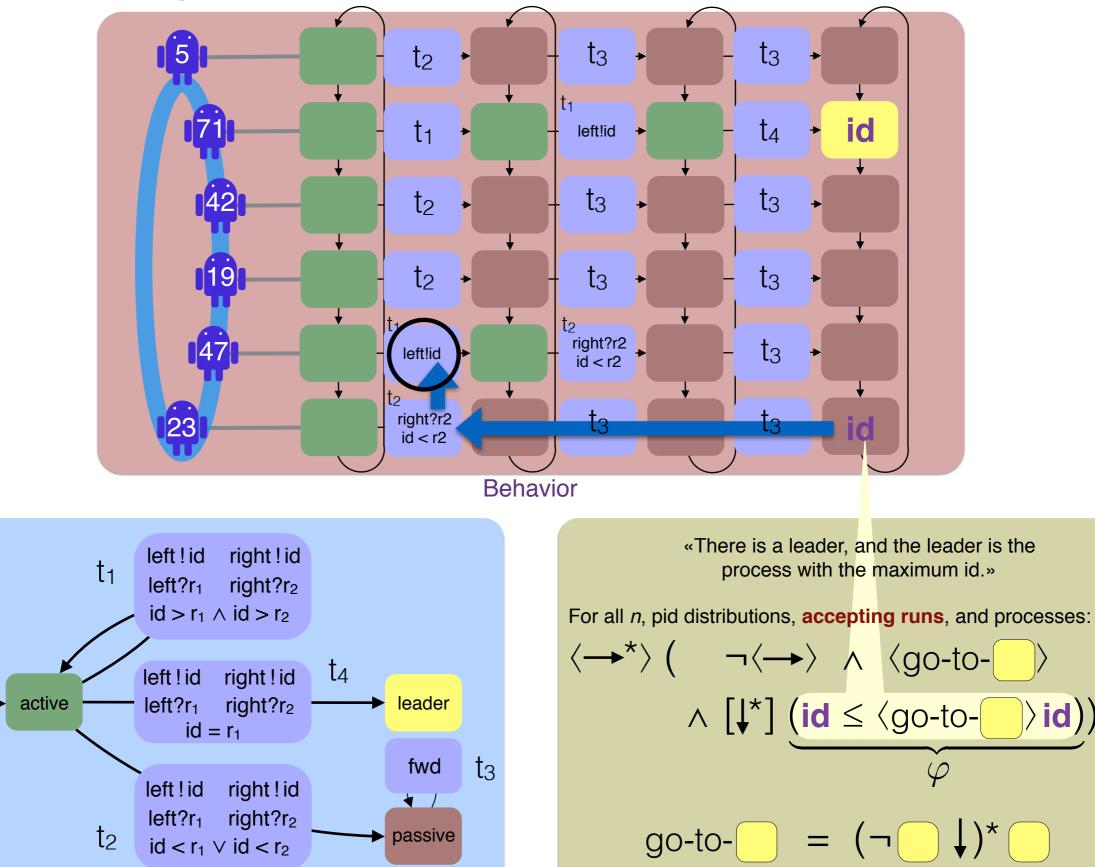
) id))



Distributed algorithm

Data PDL

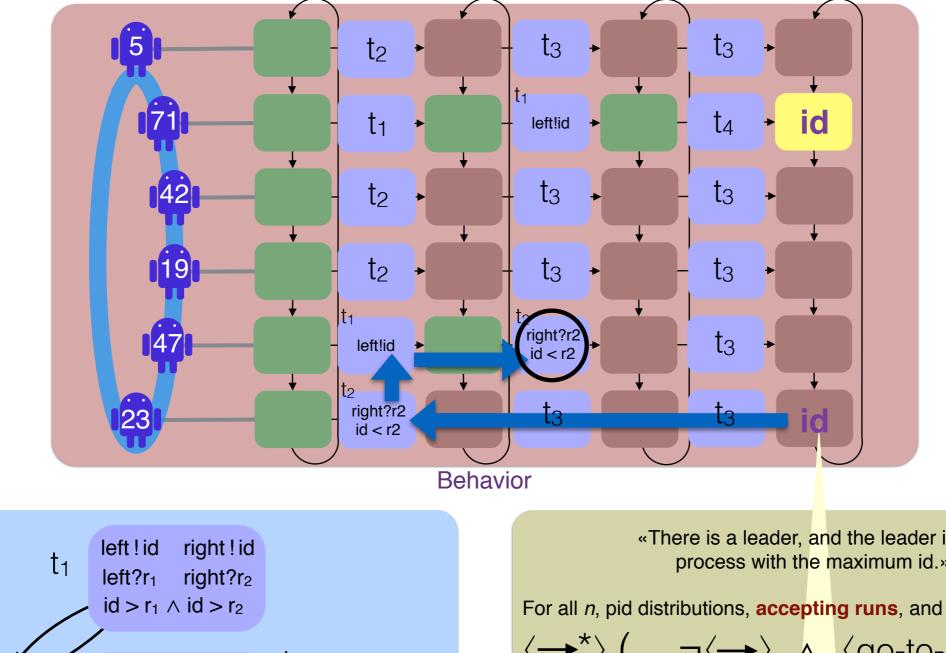
) id))



Distributed algorithm

Data PDL

) id))



$$t_1 \quad |eft ! id \quad right ! id |eft ?r_1 \quad right ?r_2 \\ id > r_1 \land id > r_2 \\ left ! id \quad right ! id |eft ?r_1 \quad right ?r_2 \\ id = r_1 \\ left ! id \quad right ! id |eft ?r_1 \quad right ?r_2 \\ id < r_1 \lor id < r_2 \\ left < r_1 \lor id < r_2 \\ left ?r_1 \lor id < r_1 \lor id < r_2 \\ left ?r_1 \lor id < r_2 \lor id < r_1 \lor id < r_2 \\ left ?r_1 \lor id < r_2 \lor id < r_1 \lor id < r_1 \lor id < r_1 \lor id < r_1 \lor id < r_2 \lor id < r_1 \lor id \lor id$$

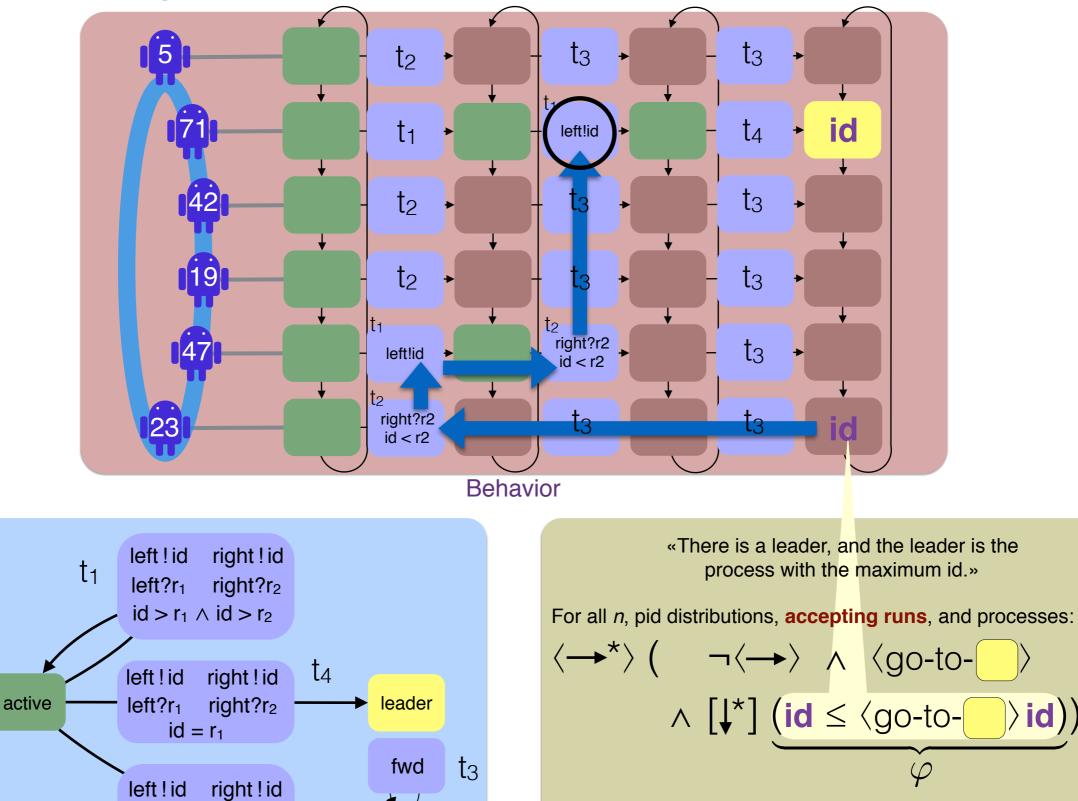
«There is a leader, and the leader is the process with the maximum id.»

For all *n*, pid distributions, **accepting runs**, and processes:

$$\langle \rightarrow^{*} \rangle \left( \neg \langle \rightarrow \rangle \land \langle \text{go-to-} \rangle \right) \\ \land [\downarrow^{*}] \left( \text{id} \leq \langle \text{go-to-} \rangle \text{id} \right) \\ \varphi \\ \text{go-to-} = (\neg \bigcirc \downarrow)^{*} \bigcirc$$

Distributed algorithm

Data PDL



4 /

passive

Distributed algorithm

left?r<sub>1</sub>

 $id < r_1 \lor id < r_2$ 

t2

right?r<sub>2</sub>

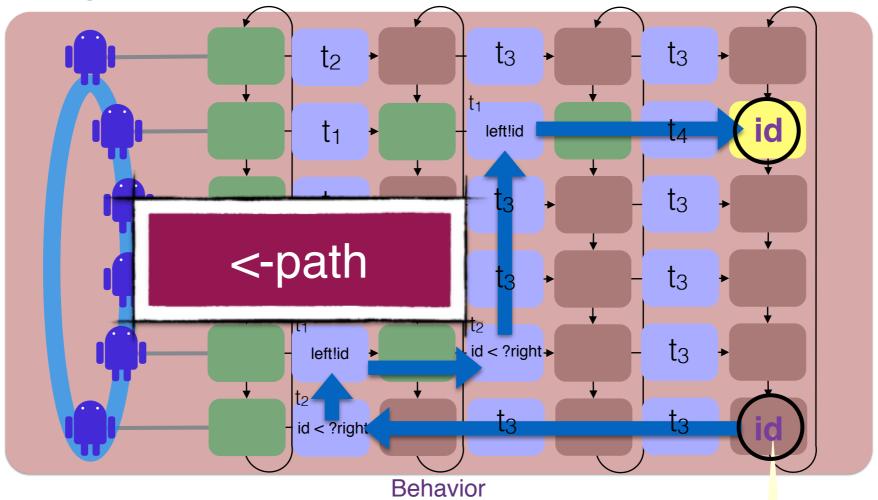
Data PDL

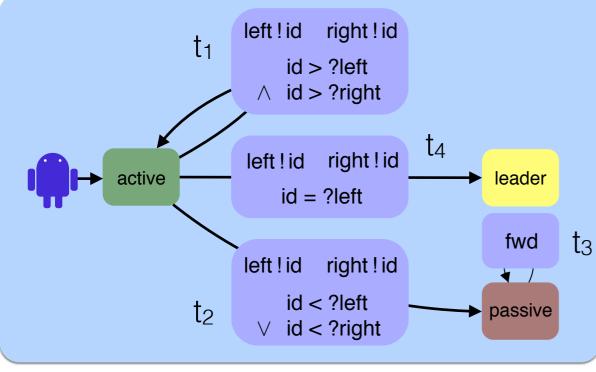
=

go-to-

⟩id))

↓)\*





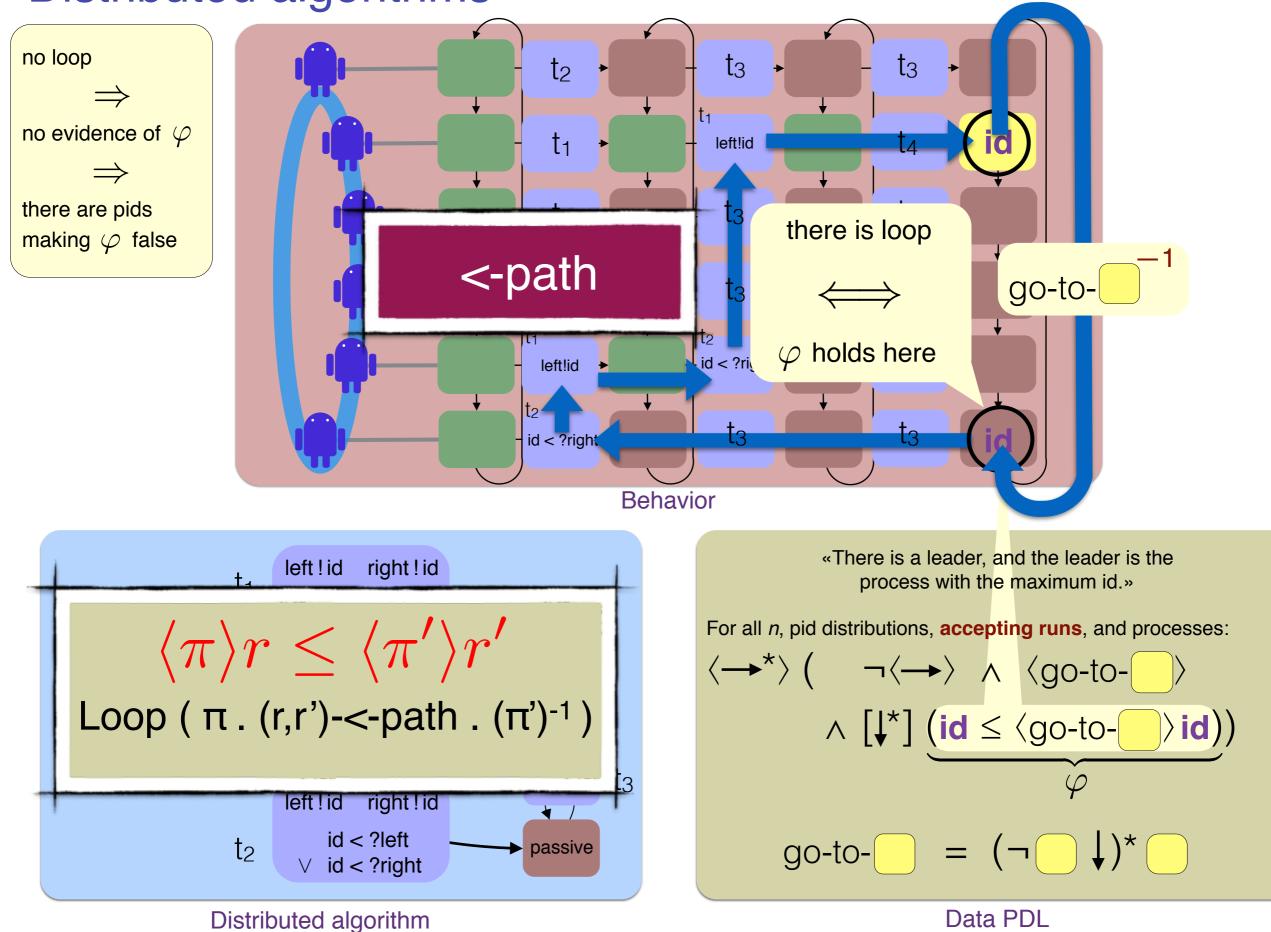
«There is a leader, and the leader is the process with the maximum id.»

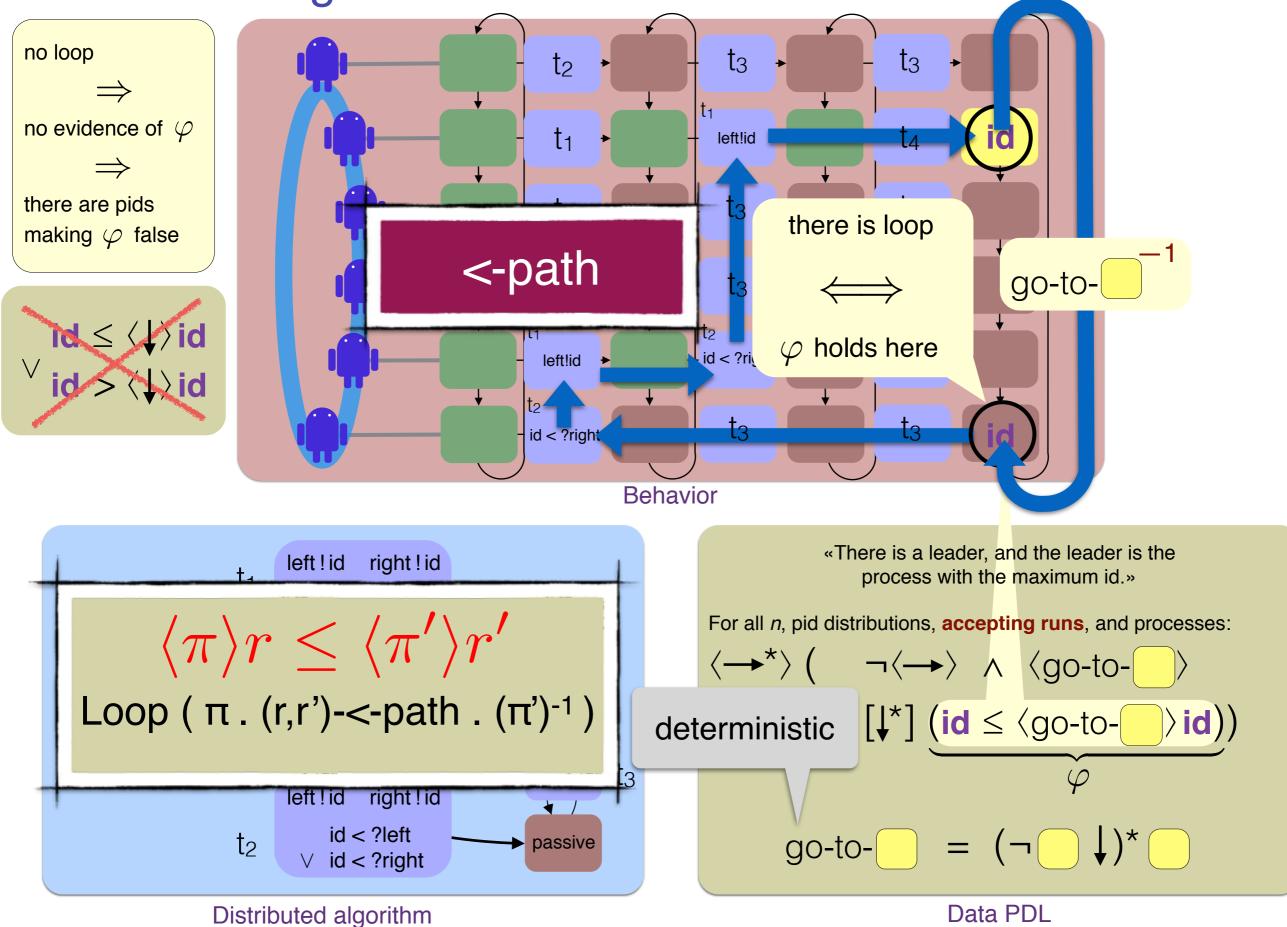
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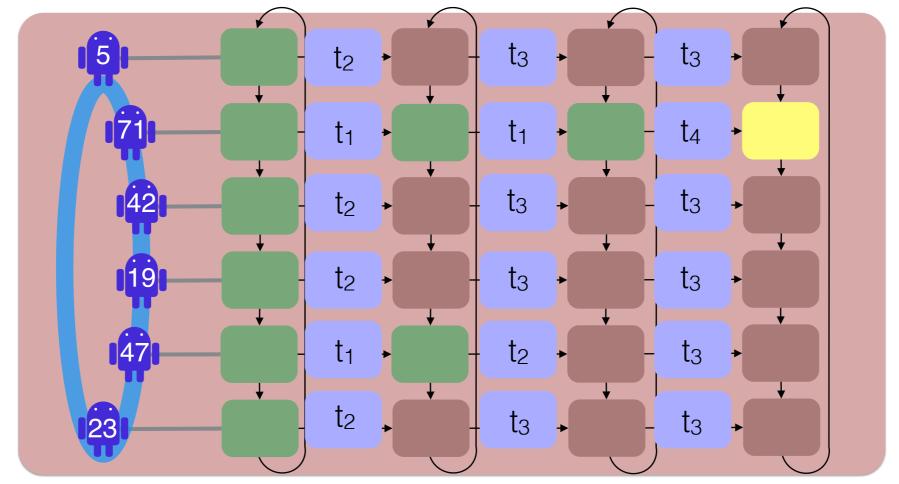
Distributed algorithm

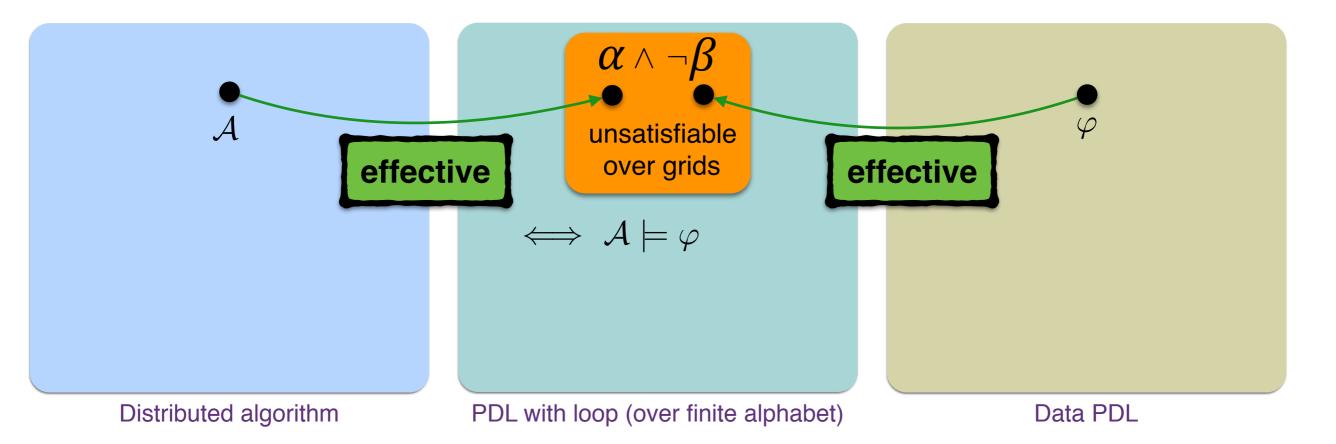
Data PDL





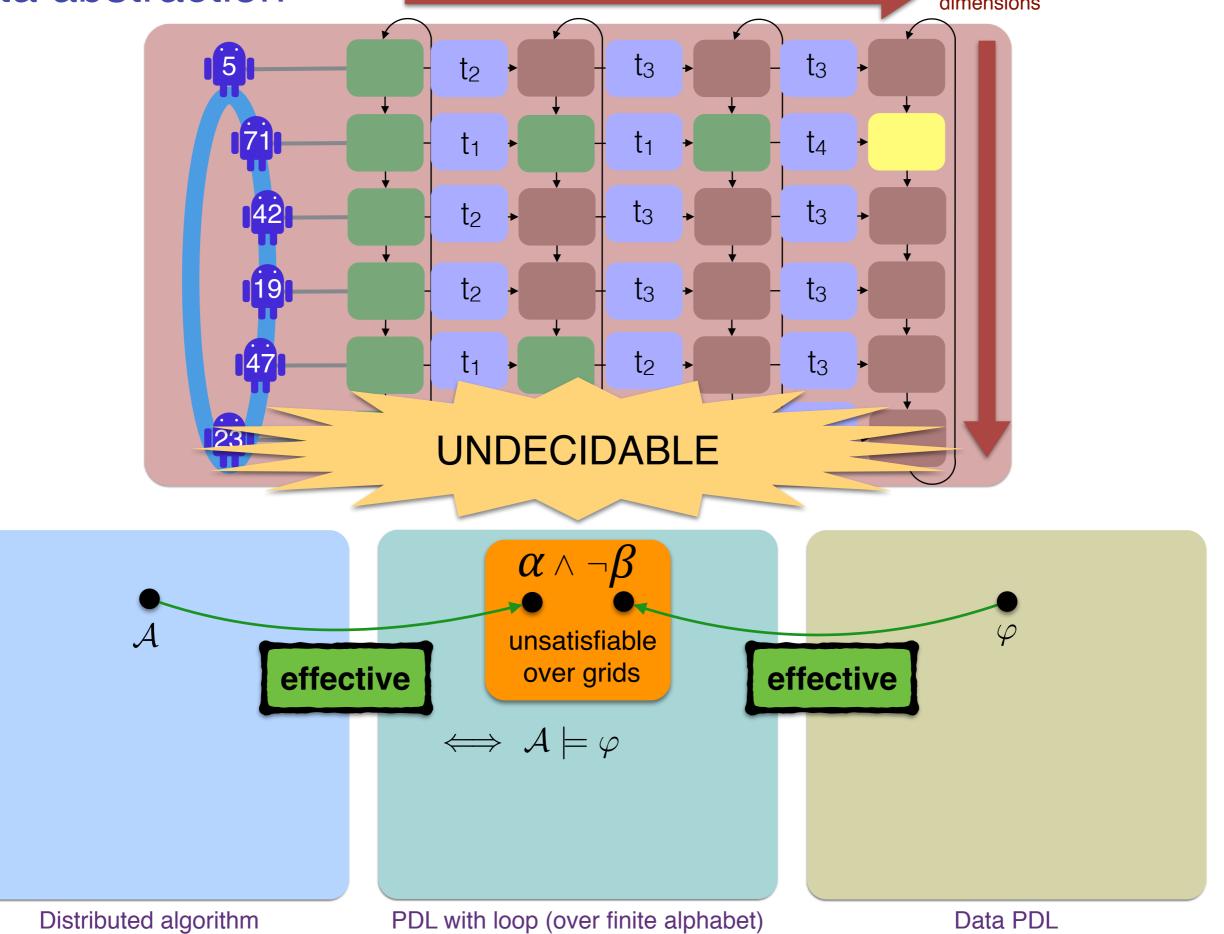
#### Data abstraction



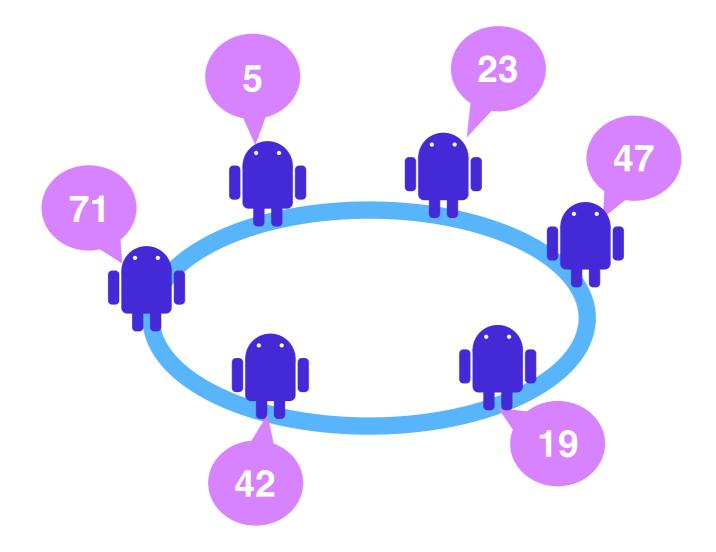


#### Data abstraction

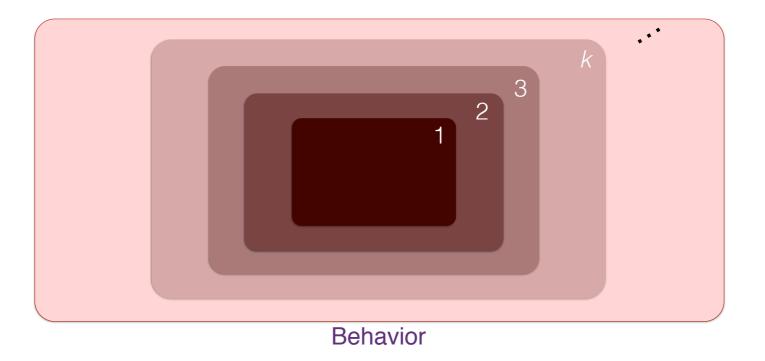
two unbounded dimensions

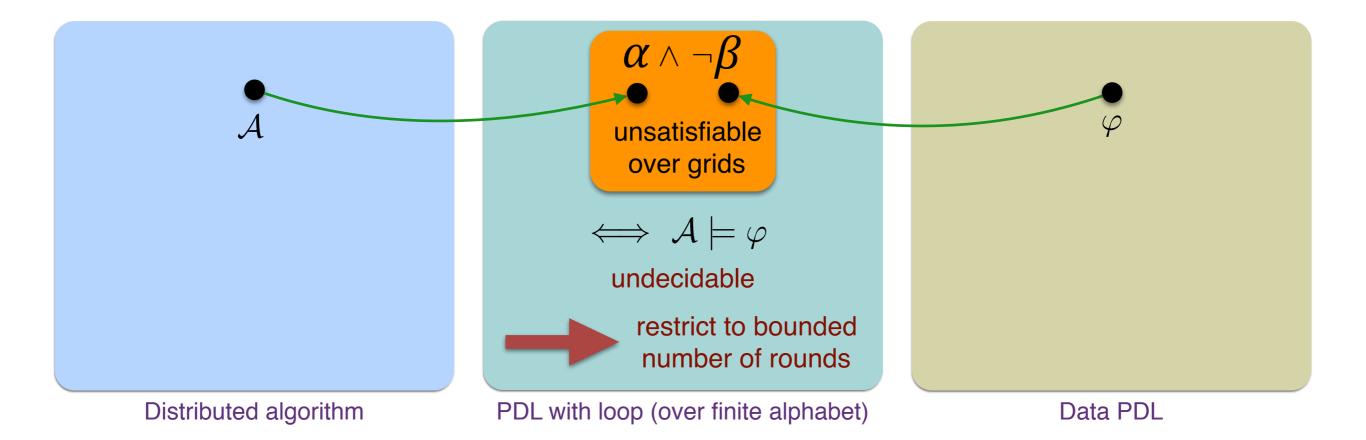


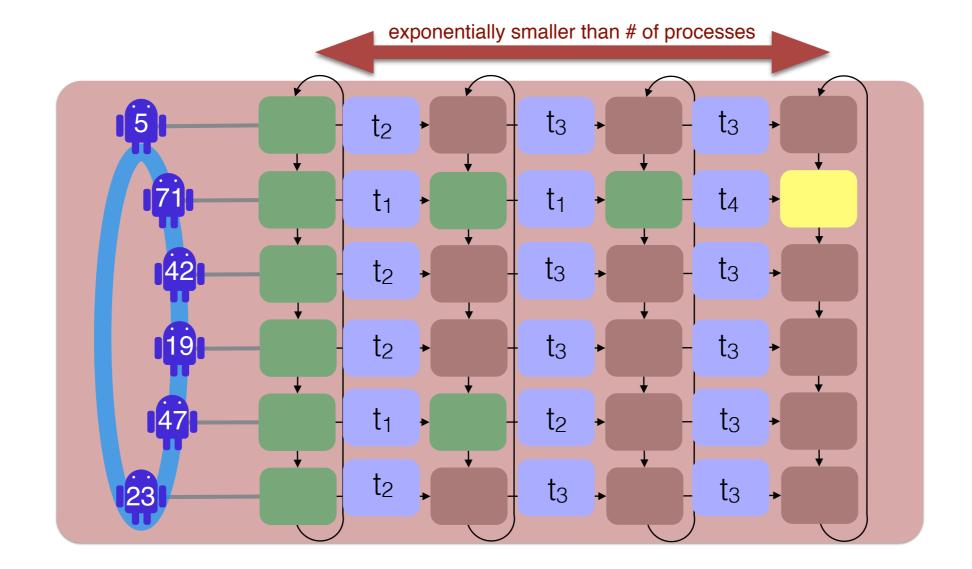
# Model Checking 2

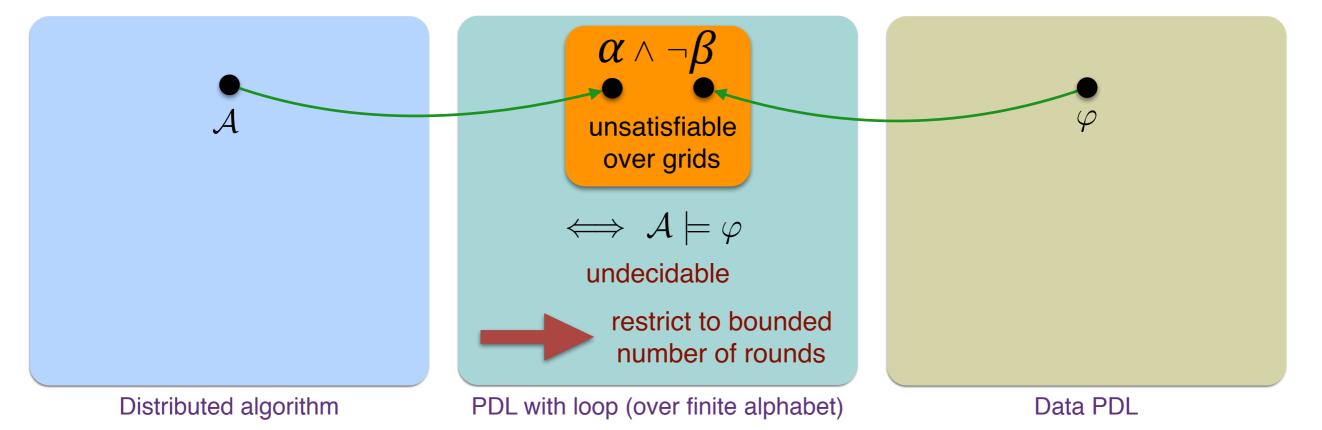


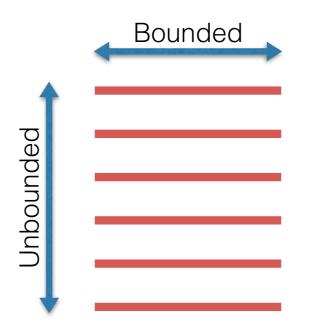
#### Under approximate verification



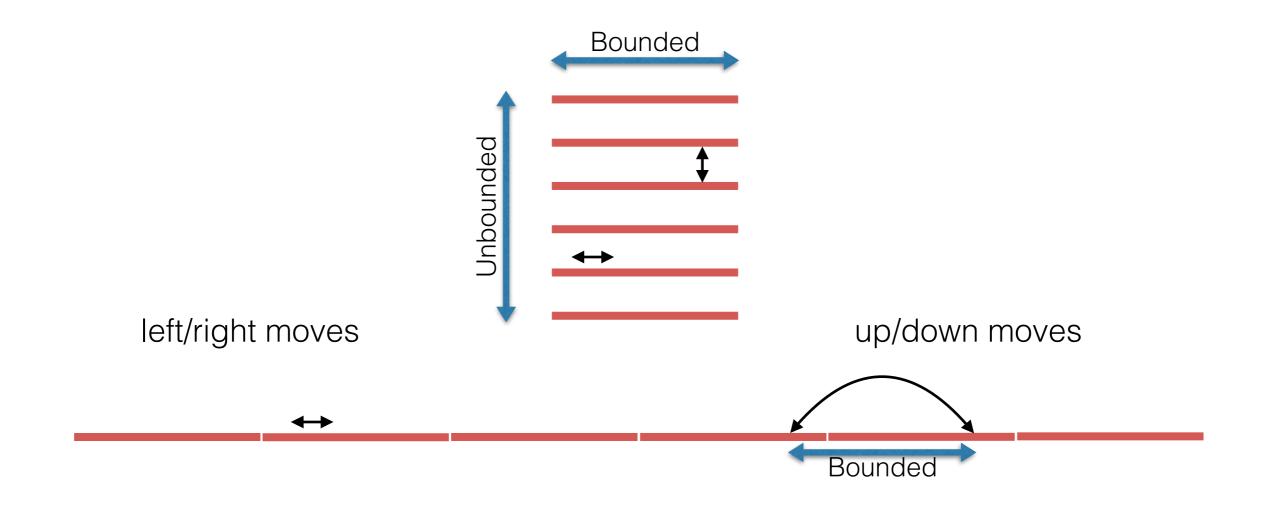




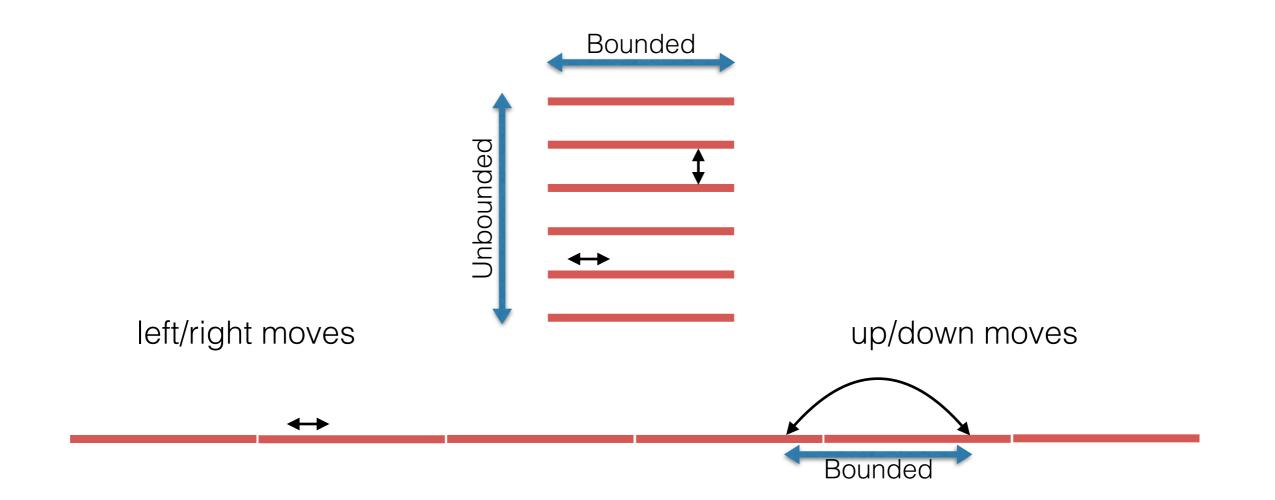


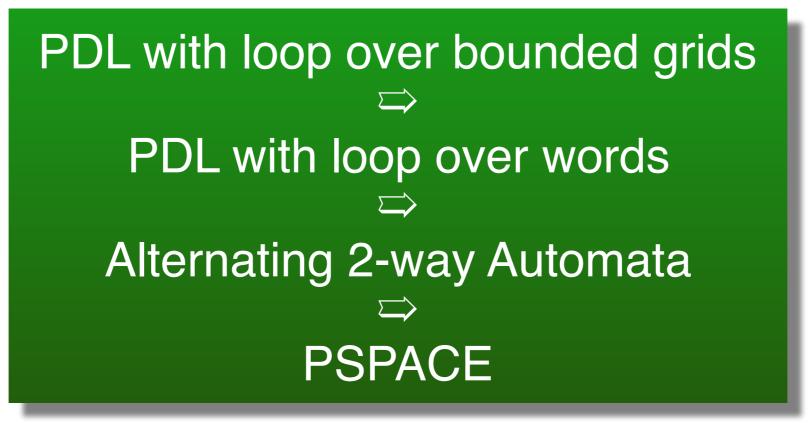


# PDL with loop over bounded grids



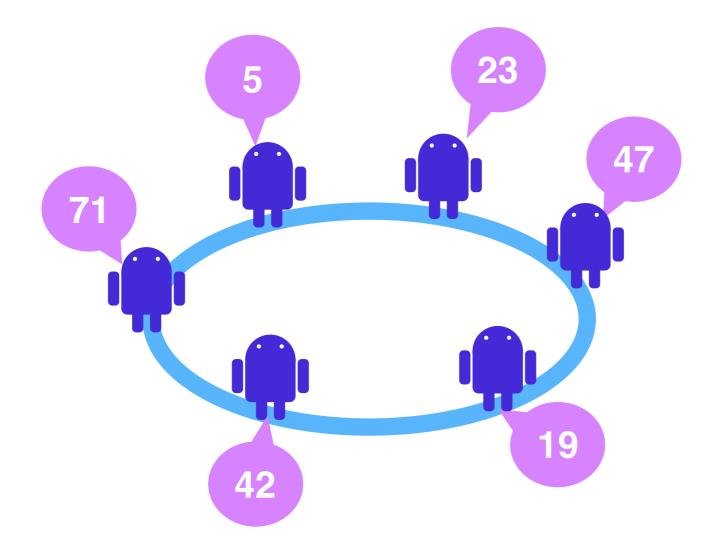
# PDL with loop over bounded grids ⇒ PDL with loop over words

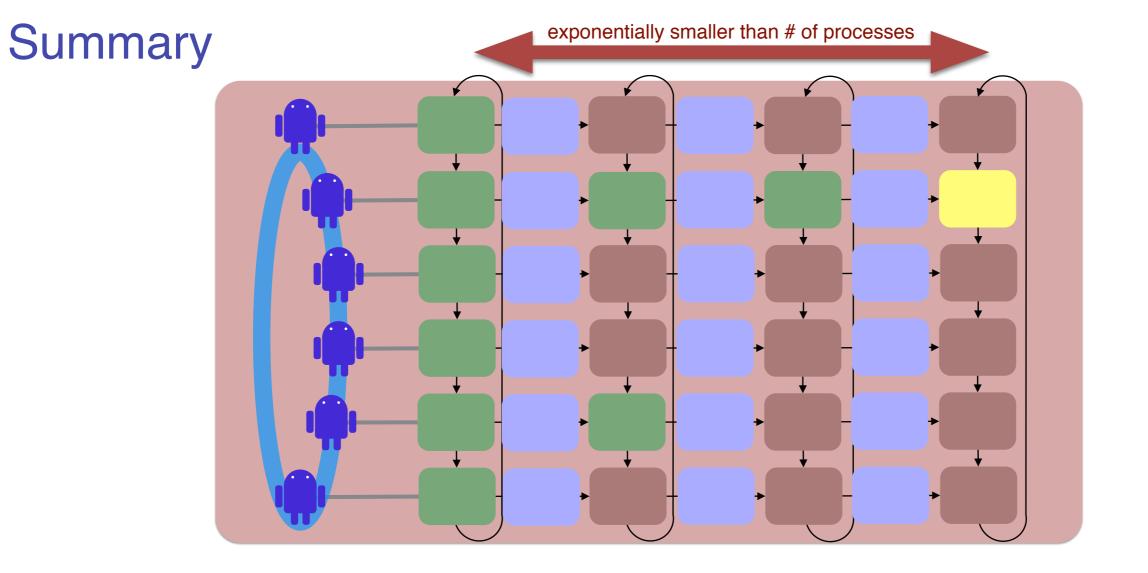




[Göller-Lohrey-Lutz '08] [Serre '08]

# **Summary & Conclusion**





Theorem (Aiswarya-Bollig-Gastin; CONCUR '15).

Round-bounded model checking distributed algorithms\* against Data PDL is PSPACEcomplete\*\*.

- \* with registers, register guards, and register updates
- \*\* unary encoding of # of rounds

# Conclusion

- What is the right temporal logic? Use generic Data PDL.
- How to deal with data?

Use symbolic technique.

**Independent of** 

- number of rounds
- restriction to rings

# Conclusion

► What is the right temporal logic? Use generic Data PDL.

Use symbolic technique.

- How to deal with data?
- How to deal with undecidability? Under-approximation.

**Independent of** 

- number of rounds
- restriction to rings

# Future work ...

- Other operations?
- Other topologies?
- Other restrictions?
- Other communications?

